A Report

DEVELOPMENT OF

AN ACTIVE FILTER SYNTHESIS PROCEDURE

SUMMARY REPORT, NAS8-5347 TP-3-83553

JUNE 23, 1964

PREPARED FOR

GEORGE C. MARSHALL SPACE FLIGHT CENTER

HUNTSVILLE, ALABAMA

PERIOD OF PERFORMANCE

20 MAY 1963 TO 20 MAY 1964

Space Craft, Inc.
8620 South Memorial Parkway
Huntsville, Alabama

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Prepared By

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ABSTRACT

This research study constitutes a joint effort by Space Craft, Inc. and the University of Alabama Bureau of Engineering Research to develop a synthesis procedure for synthesizing a four pole, four zero transfer function used for stabilization of an accelerometer control loop. Two methods of synthesizing the transfer function were investigated. The first consisted of placing networks in the control loop of an operational amplifier. Because of the complexity of the networks when used with an operational amplifier, attention was then focused toward the use of a buffer amplifier to partition the transfer function. This partitioning provided simpler transfer functions which were more easily synthesized. The part of the transfer function with real poles and zeros was synthesized by repeated zero shifting and pole removal, resulting in a ladder network. The part of the transfer function with complex zeros is synthesized by the Dasher Method. A simplified form of the synthesis procedure is presented.

Author

SUMMARY REPORT

DEVELOPMENT OF AN ACTIVE SYNTHESIS PROCEDURE

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1.0 INTRODUCTION

The purpose of this study was to develop a series of active or passive networks to be used for stabilizing a gyro accelerometer control loop. The transfer function for this control network contained four poles and four zeros with the poles being restricted to the real axis.

There were five distinct phases in the work schedule of this contract. The first was an analytical study of the system using Bode and root-locus techniques; the second was an analog computer simulation of the system; the third was a study of network synthesis methods and the development of practical electrical corrective networks; the fourth was the development of suitable buffer amplifiers and the actual fabrication and testing of the networks; and the fifth was the incorporation of the networks with the NASA accelerometer system.

Following the introduction, the Section 2 covers the general system analysis, including both the analytical and analog computer studies. Section 3 discusses the synthesis procedure used in synthesizing the networks and Section 4 introduces the use of buffer amplifiers for simplification of network partitioning. Section 5 covers the use of operational amplifiers in network synthesis and Section 6 consists of a

component survey co ing the characteristics of amplifiers and passive components. The conclusion summarizes the goals achieved and directs any further effort toward refinement of the system. Contained in the bibliography is a listing of reference material used for study and preparation of this report.

2.0 GENERAL SYSTEMS ANALYSIS

Section 2 consists of two parts—an analytical study and an analog computer study. Both of these studies were necessary before serious attention could be focused on network synthesis procedures since the form of the corrective transfer function had to be determined first. After investigating Bode, Root Locus, and Analog Computer plots, it seemed evident that a 4 pole, 4 zero transfer function satisfactorily stabilized the accelerometer system performance. Figures 1a, 1b, and 1c represent an attempt to optimize system performance. Figure 1a shows the root locus plot for the UA-6 system. Although the Bode plot is not shown, a Bode plot preceeded the root locus analysis and aided in determining the general location for the poles and zeros. In addition, the NASA Esiac analog root locus computer was used in optimizing the pole zero locations. An analog simulation of the system followed this preparatory work and the resulting output transient-response characteristics are shown on Figure 1b. Figure 1b shows that peak overshoot and settling time to an input are improved as the closed loop roots are moved outward along the root locus. Of course as the gain is increased further (beyond K = 30,000), the system becomes unstable. Although it is not shown in Figure 1b, for gains above 22,000, high frequency (500 rad/sec or so) underdamped oscillations persist. This phenomenon becomes worse as the gain is raised

UA-6 SYSTEM ROOT LOCUS

$$GH = \frac{K\left[1+\frac{s}{60}\right]\left[1+\frac{s}{200}\right]\left[1+\frac{4s}{925}+\frac{s^2}{18{,}500}\right]}{\alpha\left[s\right]\left[1+\left(\frac{s}{148}\right)^2\right]\left[1+\frac{s}{\alpha}\right]\left[1+\frac{s}{300}\right]\left[1+\frac{s}{600}\right]^2}$$

Where $\frac{K}{\alpha}$ is the open loop gain factor and is indicated on the locus for $\alpha = 1$

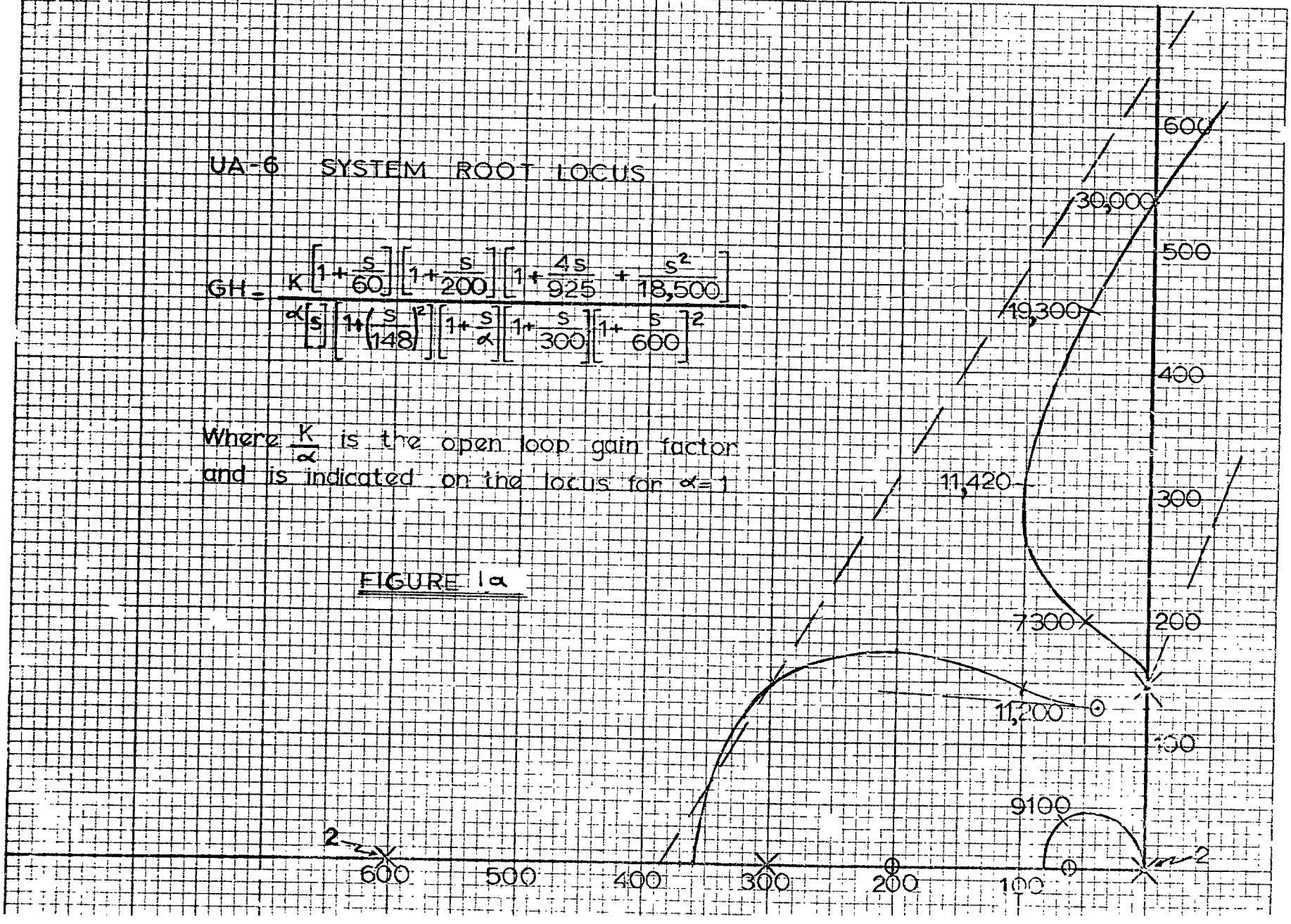


FIGURE 1a

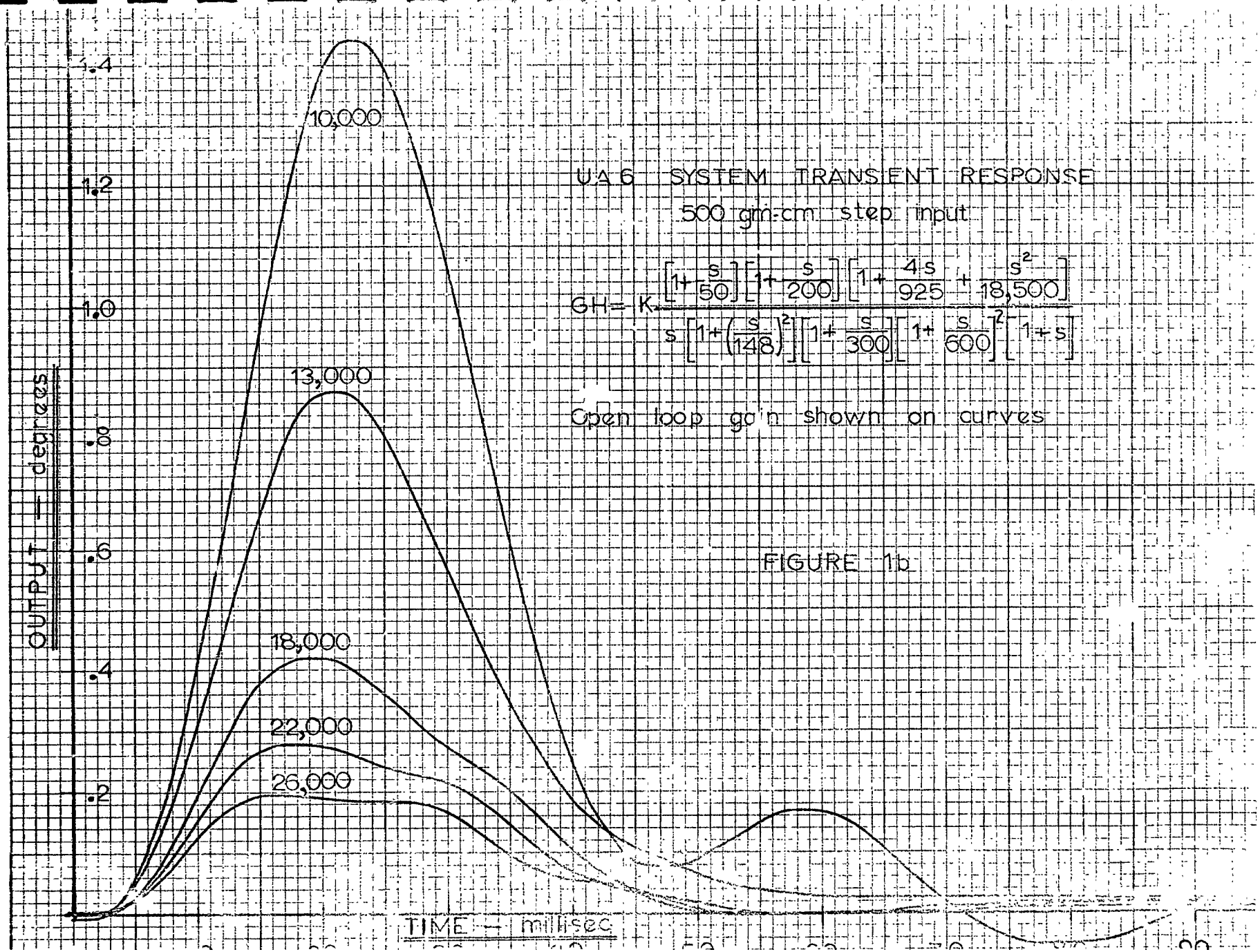
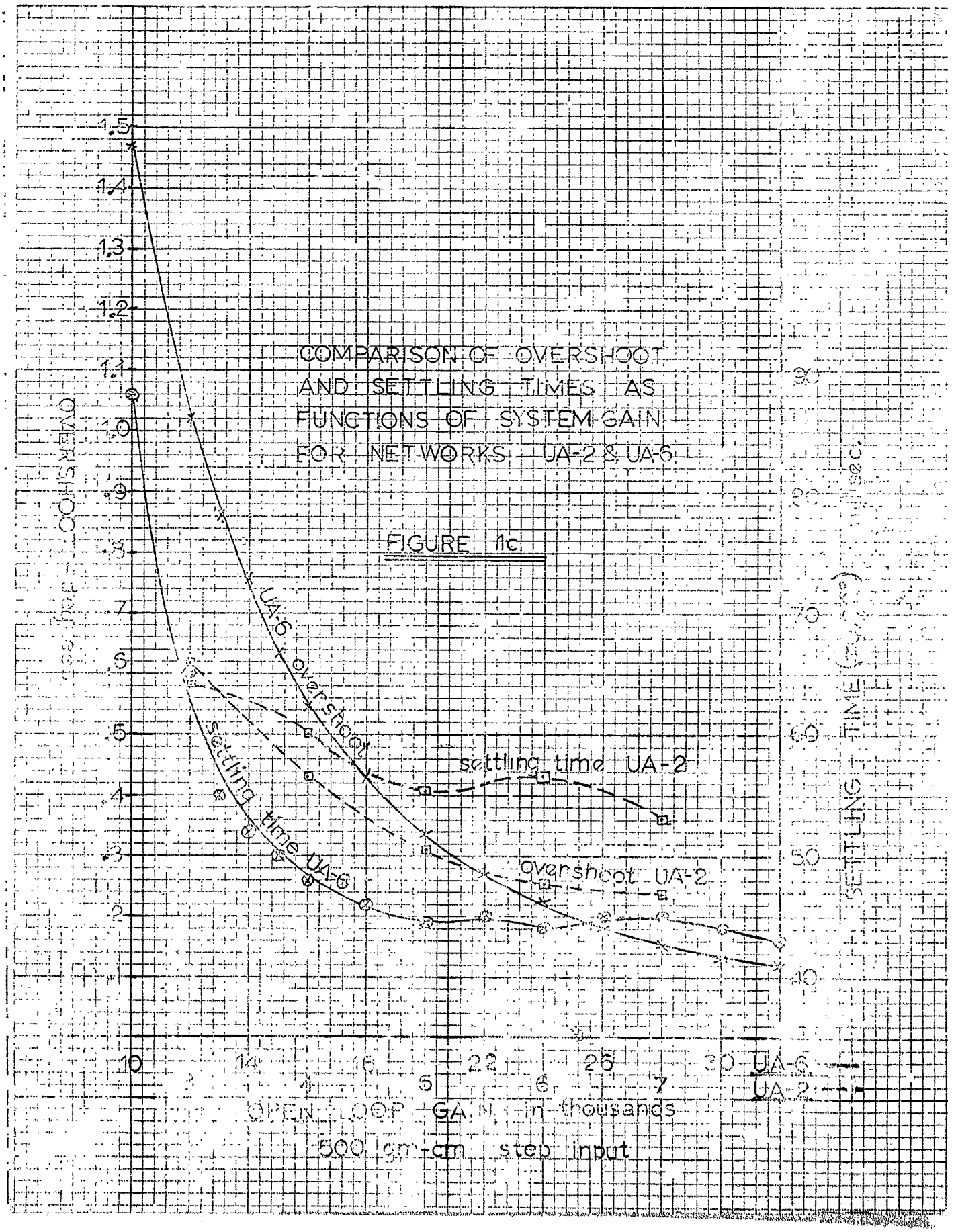

UA 6 SYSTEM TRANSIENT RESPONSE
500 gm-cm step input
$GH = K \frac{\left[1+\frac{s}{50}\right]\left[1+\frac{s}{200}\right]\left[1+\frac{4s}{925}+\frac{s^2}{18,500}\right]}{s\left[1+\left(\frac{s}{148}\right)^2\right]\left[1+\frac{s}{300}\right]\left[1+\frac{s}{600}\right]^2\left[1+s\right]}$
Open loop gain shown on curves
10,000
13,000
18,000
22,000
26,000
OUTPUT — degrees
TIME — millisec
1.4
1.2
1.0
.8
.6
.4
.2

FIGURE 1b



and instability approached.

Before proceeding with the analysis, it should be pointed out that the pole near the origin ($s = -\alpha$) is located at $s = -1$ on Figures 1a, 1b and 1c. Thus, if it is decided that a gain of 22,000 produces the most satisfactory response, but that a gain of say 44,000 is necessary, merely decrease the value of α to 0.5. The root locus and transient response characteristics remain unchanged, but the system stiffness and steady-state error are improved.

Figure 1c is included to show that a careful and perhaps exhaustive analysis of a system can result in improved system performance and that a careful analysis is therefore justified and warranted. Figure 1c shows a comparison of the UA-2 and UA-6 system characteristics as determined by an analog computer simulation. The UA-2 system was reported in Progress Report No. 3 and 4 while the UA-6 system was investigated in the latter phases of the contract work period. By a careful and judicious placement of the corrective pole-zero pattern, it was determined that the UA-6 system had a faster settling time, smaller peak overshoot, and a narrower bandwidth than the UA-2 system.

Although the UA-1, UA-2, UA-3, UA-5 and UA-6 systems are mentioned in this and, except for the UA-6 system, in earlier Mon-

thly Progress Reports, the UA-4 system receives the most attention in this Final Report. The reason for this emphasis is that a particular transfer function had to be developed rather early in the contract study in order to proceed with the network synthesizing and the fabrication and testing. The UA-4 system represents a safe, stable system and results in a system performance somewhere between the UA-2 and UA-6 systems.

The corrective networks for the UA-4 system were designed in a variety of configurations; i. e., all R-C passive networks, one buffer amplifier plus passive networks, two buffer amplifier plus passive networks, and the operational amplifier plus passive networks. In addition, the various networks were designed to produce d-c open loop gains from 5,000 to 500,000.

Since primary attention was to be focused on the use of passive networks and not on the operational amplifier approach to network synthesis, it was necessary to have at least as many poles as zeros in the corrective transfer function. Should the operational amplifier approach prove to be feasible at some later date, it should be noted that with it one can reproduce almost any transfer function with relative ease. The techniques for using operational amplifiers are developed in Section 5.

It was decided early in the work schedule to use resistors and capacitors but not inductors in the corrective networks. This choice was made for three reasons: (1) inductors are not as idealized circuits elements as are capacitors and resistors; (2) resistors and capacitors can be obtained as off-shelf items in a wide variety of component values but inductors cannot; and (3) it is easier to develop the network synthesis procedures for the R-C rather than the R-L-C situation. The primary consideration for choosing R-C circuits was based on the first two reasons.

After a commitment was made to work with only R-C networks, it was necessary to develop a corrective transfer function with poles on the real axis only. After many trial and error approaches, it was found that a 4-pole 4-zero transfer function gave satisfactory system performance. The analysis was greatly facilitated by the use of one of NASA's ESIAC computers.

In light of the excellent results obtained, there is no reason to change this viewpoint and in fact, additional effort could be profitably spent in investigating further R-C active and passive network synthesis. The authors do feel, however, that the use of RLC circuits is justifiable in some situations and certainly do not wish to recommend ignoring this potentially fruitful area.

The restriction of only R-C networks forced the poles of the corrective transfer function to be located on the negative real axis of the s plane. After a careful analytical analysis of the system response, it was determined that the real-axis pole restriction was really quite satisfactory. Although exhaustive calculations using complex poles were not made, preliminary investigations did indicate that complex poles in the corrective transfer function would not be particularly desirable over real-axis poles. Thus, in using R-C rather than RLC networks, the choosing of real-axis pole locations was therefore almost mandatory.

An analog computer simulation of the overall accelerometer system, including the corrective transfer function, confirmed that the transient response would be satisfactory. The analog computer results are shown in Section 2.2.

Several corrective transfer functions were developed during the course of the investigation. These transfer functions and associated networks were labeled by UA-1, UA-2, UA-3, UA-4, UA-5, UA-6, etc. designations. The system root locus plots typified by these corrective transfer functions fell into two distinct patterns. These two patterns are illustrated by the root locus plots shown in Figures 4 and 5, which represent the UA-4 and UA-6 systems, respectively. The open loop

transfer function for the UA-4 system is

$$GH(s) = \frac{K}{\alpha} \frac{\left[1+\frac{s}{82}\right]\left[1+\frac{s}{184}\right]\left[1+\frac{1}{194}s+\frac{1}{19{,}400}s^2\right]}{s\left[1+\left(\frac{s}{148}\right)^2\right]\left[1+\frac{s}{\alpha}\right]\left[1+\frac{s}{300}\right]\left[1+\frac{s}{1000}\right]\left[1+\frac{s}{1200}\right]} \qquad (1)$$

and for the UA-6 system is

$$GH(s) = \frac{K}{\alpha} \frac{\left[1+\frac{s}{60}\right]\left[1+\frac{s}{200}\right]\left[1+\frac{4}{925}s+\frac{1}{18{,}500}s^2\right]}{s\left[1+\left(\frac{s}{148}\right)^2\right]\left[1+\frac{s}{\alpha}\right]\left[1+\frac{s}{300}\right]\left[1+\frac{s}{600}\right]^2} \qquad (2)$$

Or in root form the transfer functions are

$$GH(s) = A\frac{(s+82)(s+184)\left(\overline{s+50}^2+130^2\right)}{s(s^2+148^2)(s+\alpha)(s+300)(s+1000)(s+1200)} \qquad (1a)$$

and

$$GH(s) = A\frac{(s+60)(s+200)\left(\overline{s+40}^2+\overline{130}^2\right)}{s(s^2+148^2)(s+\alpha)(s+300)(s+600)^2} \qquad (2)$$

The root locus plot for the UA-4 system is similar to the UA-1 system described in Monthly Progress Report 3 and 4, while the root locus plot for the UA-6 system is similar to the UA-2 system which is also described in Monthly Progress Report 3 and 4.

The UA-6 system was analyzed and synthesized on an analog computer but the UA-4 system was tested in actual practice. The

bulk of this report is concerned with the corrective transfer function described by the UA-4 system. The reason for this is because the UA-4 system is rather insensitive to network parameter variations in that the poles and zeros could shift by 10 to 30 percent without materially affecting the system performance.

The UA-6 transfer function was developed in an attempt to optimize the system performance in regard to such considerations as peak overshoot, bandwidth, and settling time. All system performance characteristics of the UA-6 system were improved over those of the UA-4 system. The bandwidths were 740 rad/sec, and 460 rad/sec, the peak overshoots were 0.26 degrees and 0.22 degrees and the settling times to within 0.02 degrees were 56 and 44 milliseconds for a 500 gm-cm input and an open loop gain of 25,000 for the UA-4 and UA-6 systems, respectively. Had time permitted, the UA-6 networks could have been fabricated and tested in the NASA accelerometer system as were the UA-4 networks.

2.1 Analytical Studies

Before beginning the synthesis of a corrective network, the necessary corrective transfer function must be developed. As usual it is a trial and error process to find the optimum transfer function that gives the best system performance.

The block diagram of the accelerometer, the associated electronics, and corrective network is shown in Figure 2.

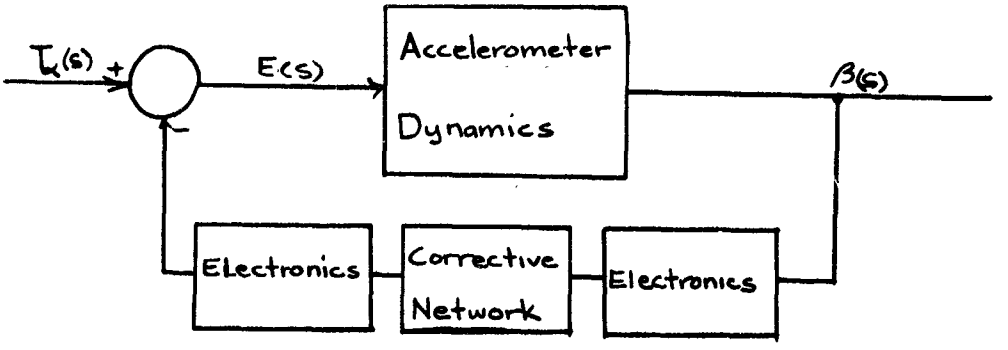


Figure 2. Block Diagram of Corrected Accelerometer System.

The accelerometer transfer function is

$$\frac{\beta(s)}{E(s)} = \frac{148^2/110}{s(s^2+148^2)} \tag{3}$$

for the particular accelerometer that was stabilized in this study.

It can be assumed that the electronic circuits noted on either side of the corrective network in Figure 2 contribute only a magnitude gain factor and that the corrective network contributes both gain and phase shift properties. Several corrective network transfer functions were investigated and reported on in previous monthly reports. All of these transfer functions were

of the form

$$H(s) = T_{12}(s) = K_1 \frac{(s+\sigma_1)(s+\sigma_2)(\overline{s+\sigma_o}^2 + \omega_o^2)}{(s+\sigma_3)(s+\sigma_4)(s+\sigma_5)(s+\sigma_6)} \tag{4}$$

During the analysis of the overall system performance the poles and zeros in Equation 4 were given several different values. A typical set of values is given in Equation 5.

$$H(s) = K_1 \frac{(s+82)(s+184)(\overline{s+50}^2 + 130^2)}{(s+\alpha)(s+300)(s+1000)(s+1200)} \tag{5}$$

The network resulting from the synthesis of Equation 5 is referred to as the UA-4 network in the previous monthly reports. Combining Equations 3 and 5 the overall open loop transfer function becomes

$$GH(s) = K \frac{(1+\frac{s}{82})(1+\frac{s}{184})(1+\frac{1}{194}s+\frac{1}{19400}s^2)}{s\left[1+(\frac{s}{148})^2\right](1+\frac{s}{\alpha})(1+\frac{s}{800})(1+\frac{s}{1000})(1+\frac{s}{1200})} \tag{6}$$

in time constant form. The K term is the open loop d-c gain factor and α is a pole near the origin such that $0 \leq \alpha \leq 10$ for all discussions and analyses in this report.

In root form Equation 6 becomes

$$GH(s) = A \frac{10^{\beta}(s+82)(s+184)(\overline{s+50}^2 + 130^2)}{s(s^2+148^2)(s+\alpha)(s+300)(s+1000)(s+1200)} \tag{7}$$

The root locus plot for Equation 7 is shown in Figure 3b. The shape of the root locus is insensitive to changes in the value of α for α between zero and about 10; however, the gain calibration is definitely a function of α. Note that a comparison of Equations 6 and 7 relates A and K by letting s = 0 in both equations and equating or

$$K = \frac{A \cdot 10^8 \cdot 82 \cdot 184 \cdot 19400}{\alpha \cdot 148^2 \cdot 300 \cdot 1000 \cdot 1200}$$

$$K = \frac{3710A}{\alpha} \tag{8}$$

The term K equals K_V which is called the velocity error coefficient, which in turn determines the system steady state error to a velocity input. In order to minimize this steady state error and thus increase system "stiffness" one can increase the amplifier gain and reduce α. To increase amplifier gain without changing α causes the closed loop poles to shift to new locations which may result in unsatisfactory system operation. If the amplifier gain is increased and α decreased a proportional amount, the closed loop poles remain fixed and K or K_V is increased (this is because α is near the origin). As an example, suppose it is desirable to achieve an open-loop gain factor K of 25,000. After a study of the root locus plots, Bode plots, and perhaps an analog simulation, suppose one decides to place a closed loop pole at

UA-4 SYSTEM ROOT LOCUS

$$GH = \frac{K}{\alpha}\,\frac{\left[1+\frac{S}{82}\right]\left[1+\frac{S}{184}\right]\left[1+\frac{S}{194}+\frac{S^2}{19400}\right]}{S\left[1+\frac{S}{\alpha}\right]\left[1+\left(\frac{S}{148}\right)^2\right]\left[1+\frac{S}{300}\right]\left[1+\frac{S}{1000}\right]\left[1+\frac{S}{1200}\right]}$$

WHERE $\frac{K}{\alpha}$ IS THE OPEN LOOP GAIN FACTOR AND IS SHOWN ON THE ROOT LOCUS FOR $\alpha = 1$

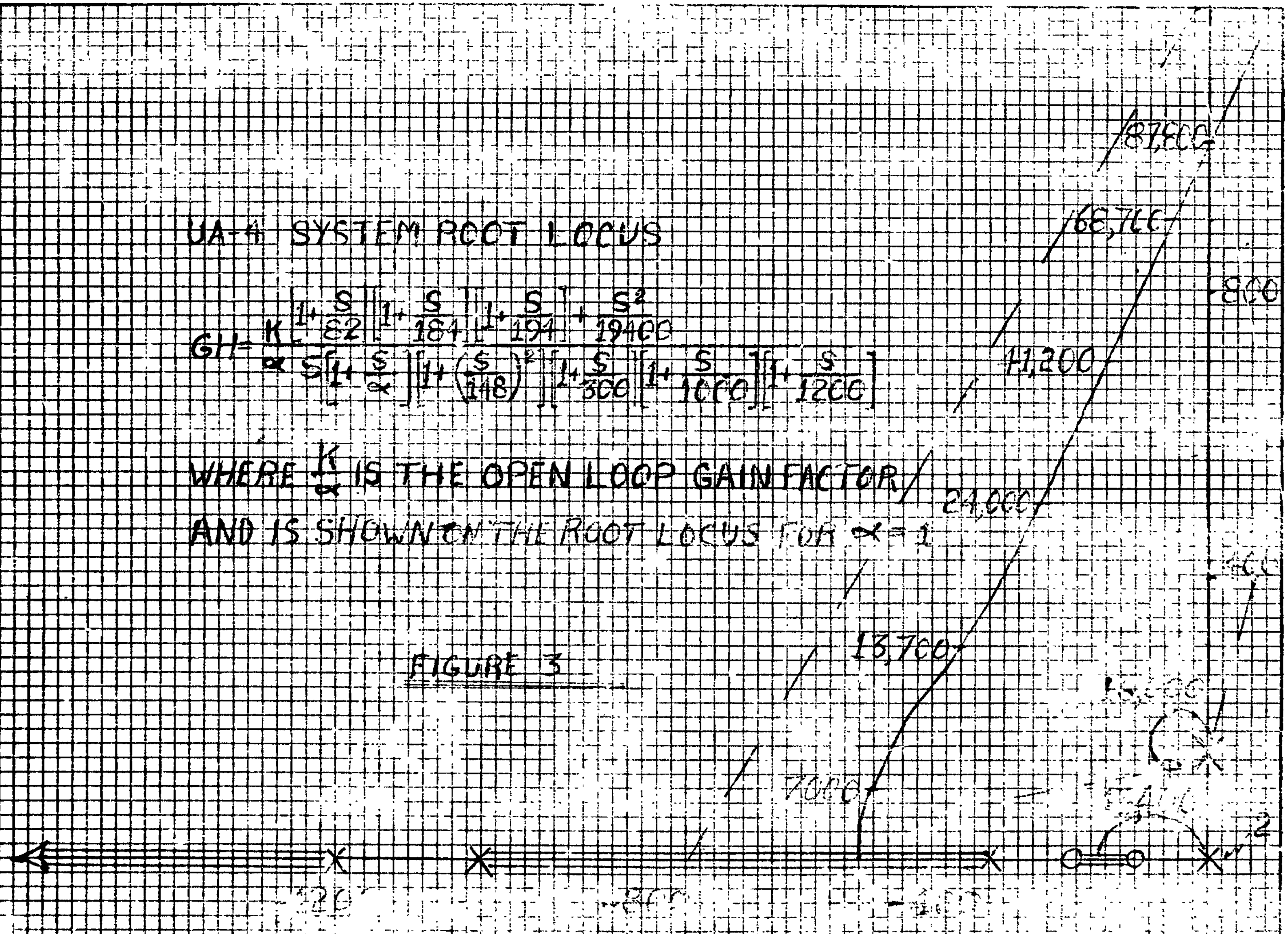


FIGURE 3

s = 100 + j 800 (assume that the other corresponding closed loop pole locations are satisfactory). According to Figure 3, a root at this location requires K to equal 55,000 for $\alpha = 1$. One can determine the required value for α by the relation

$$K(\alpha) = \frac{K(\alpha=1)}{\alpha}$$

or

$$\alpha = \frac{55,000}{25,000} = 2.2$$

From a Bode plot analysis, the 0 db crossover frequency or bandwidth is about 740 rad/sec for the transfer function defined by Equation 6. From analog computer studies the system performance was expected to be satisfactory and from actual tests on NASA's accelerometer system, the performance tests were indeed gratifying.

As pointed out in Monthly Progress Report 8, networks were developed from tne transfer function defined by Equation 5 for α = 0.1, 1, 2.5, 5 and 10 and networks for α = 2 were shown in Report 10 and 11. These networks resulted in system loop gain factors of 500,000, 50,000, 20,000, 10,000, 5,000 and 25,000, respectively. Networks which reproduced the desired transfer function with the above mentioned values for α were designed by the University of Alabama researchers and fabricated

by Space Craft personnel. The networks were either passive or active in nature with the active network using either buffer or operational amplifiers as the active element. Without fail every network inserted in the system resulted in a safisfactory stabilization of the accelerometer.

After the system analysis provided insight as to what the form of the transfer function should be for the corrective network, synthesis of a suitable network was begun. The synthesis techniques and developments are given in Sections 3, 4 and 5 of this report.

2.2 Analog Computer Simulation

In order to compare the transient response of the Gyro with different compensation networks, the system was simulated on the analog computer. Here is an explanation of the simulation with one compensation network.

The forward loop simulation:

$$G(s) = \frac{C}{E}(s) = \frac{\frac{1}{110}\left(\frac{\text{rad.}}{\text{gm.cm}}\right)}{S\left(\frac{s^2}{129.7^2}+1\right)\left(\frac{s^2}{2260^2}+1\right)} = \frac{4.48\times10^{10}\left(\frac{\text{deg.}}{\text{gm.cm}}\right)}{(s^2+129.7^2)(s^2+2260^2)S} \quad (9)$$

Define

$$G(s) = G_1(s)\,G_2(s) = \frac{C}{Y}\,\frac{Y}{E}(s)$$

where $\frac{Y}{E}(s) = G_1(s) = \frac{129.7 \times 10^6}{s(s^2+129.7^2)}$

and $\frac{C}{Y}(s) = G_2(s) = \frac{3.454 \times 10^4}{s^2+2260^2}$

$\frac{Y}{E}(s) = G_1(s)$ can be expanded and solved to yield

$$Y(s) = 129.7 \times 10^6 \frac{E}{s^3} - 129.7^2 \frac{Y}{s^2} \qquad (10)$$

This is realized by the following computer circuit.

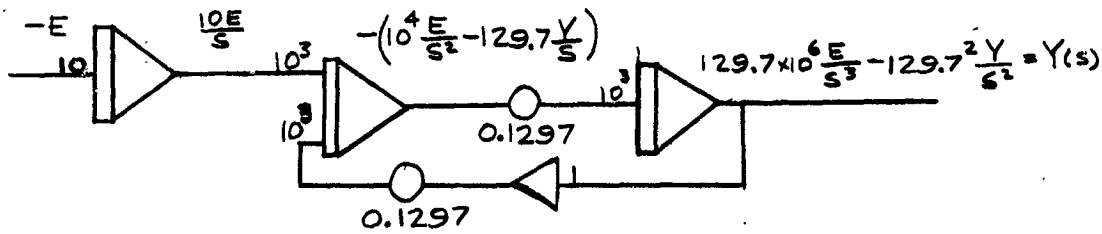


Figure 4. Circuit to Realize Y(s)

$$\frac{C}{Y} = G_2(s) = \frac{3.454 \times 10^4}{s^2 + 2260^2} \tag{11}$$

this can be expanded and solved to give

$$C(s) = 3.454 \times 10^4 \frac{Y}{s^2} - 2260^2 \frac{C}{s^2} \tag{12}$$

This $C_{(s)}$ is realized by the following computer circuit

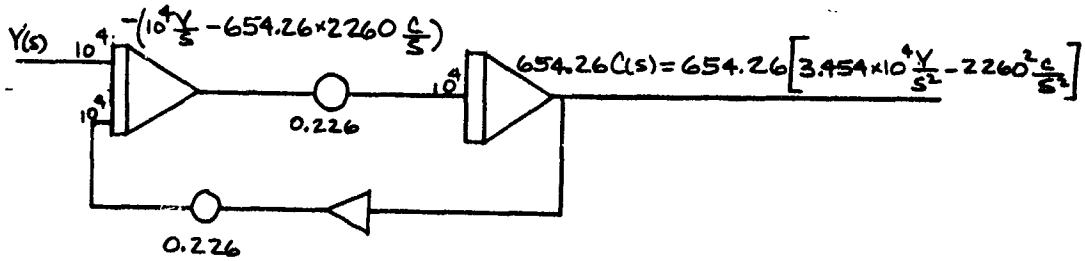


Figure 5. Circuit to Realize $C_{(s)}$

The 654.26 being a convenient scaling factor.

The feedback loop simulation:

The feedback loop simulated here is

$$\frac{B}{C}(s) = H(s) = K \frac{(s+82.2)(s+184.4)(s+847)\left[(s+51.4)^2 + 129.7^2\right]}{(s+6.2)\left[(s+287)^2 + 174^2\right]\left[(s+372)^2 + 1358^2\right]} \tag{13}$$

K was chosen as 65.400 to give a maximum open loop gain of 6289.

Since a gain excess of 654.26 has been realized in the forward loop, the simulation of the Feedback will be

$$\frac{B}{C} = \frac{65400}{654.26}\left[\frac{(s+82.2)---}{(s+6.2)---}\right] = 100\left[\frac{(s+82.2)---}{(s+6.2)---}\right] \quad (14)$$

the Feedback transfer function is broken down as follows

$$100\,\frac{(s+82.2)(s+184.4)(s+847)\left[(s+51.4)^2+129.7^2\right]}{(s+6.2)\left[(s+287)^2+174^2\right]\left[(s+372)^2+1358^2\right]} = K'H_1(s)H_2(s)H_3(s) \quad (15)$$

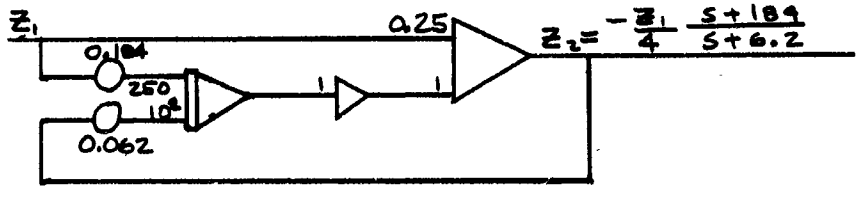
where $K' = 100$

$$H_1(s) = 0.25\,\frac{s+184.4}{s+6.2}$$

$$H_2(s) = \frac{(s+82.2)(s+847)}{(s+372)^2+1358^2}$$

$$H_3(s) = 4\,\frac{(s+51.4)^2+129.7^2}{(s+287)^2+174^2}$$

The Feedback Simulation was realized as follows



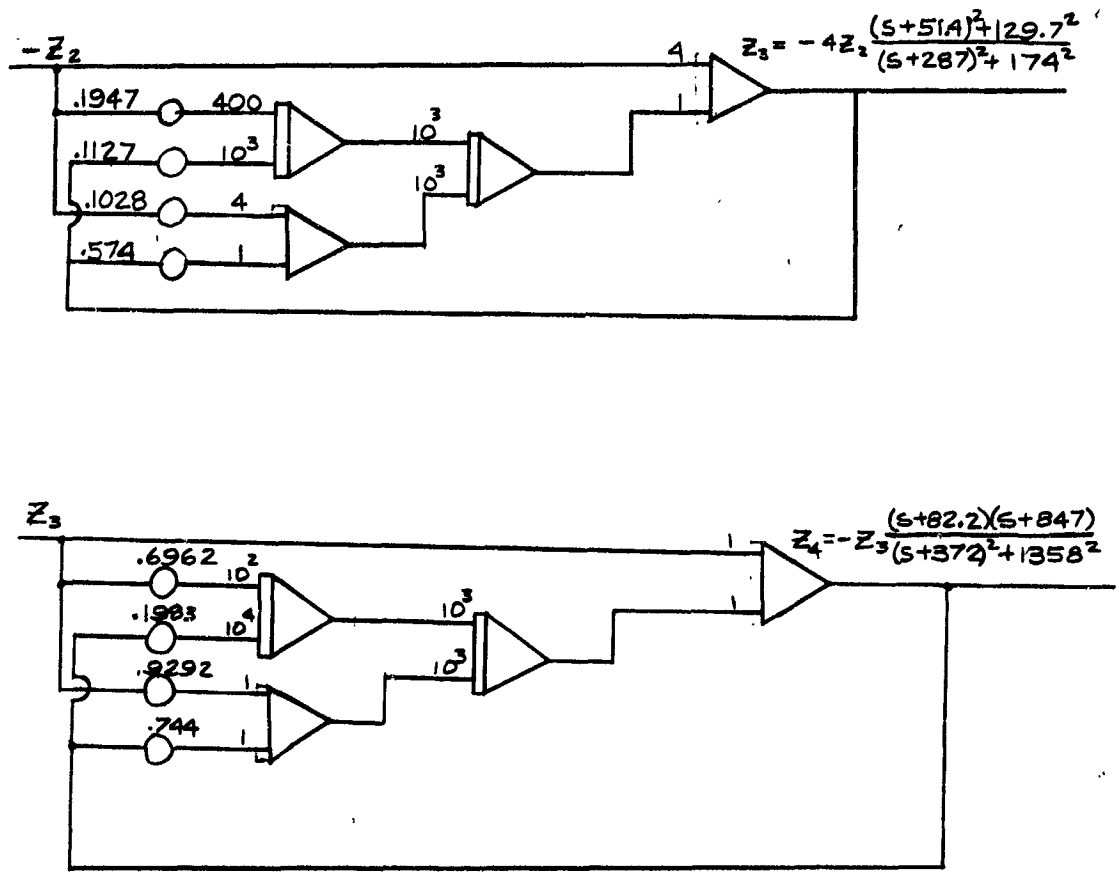
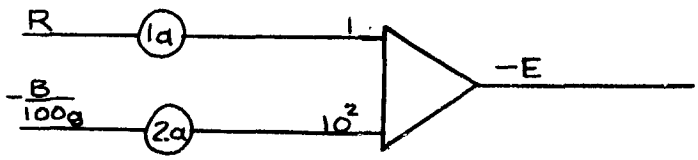


Figure 6. Circuits to Realize Feedback Simulation

The gain K = 100 is realized on the error summing amplifier



Pot 2a can be set to any value g to give desired open loop gain.

For example g = 1 (KGH) = 6289

g = 0.796 (KGH) = 5000

The computer may be slowed down (time scaled) by lowering all integrator gains by the desired time scale factor. In this case all integrator gains were slowed by a factor of 10^3.

The results were interpreted as follows:

100 volts out of the forward loop was equated to 2°. The dc gains of the feedback simulation is 14.65 when the open loop gain is 5000.

For an open loop gain of 5000, the actual system feedback gain is 9,570 grcm/degree.

Thus 1° is represented by 50 volts gives 14.65 x 50 = 732.5 volts for B.

But 1° x 9570 grcm/degree = 9,570 grcm

thus 732.5 volts represents 9570 grcm

or B is scaled at $\frac{9570}{732.5}$ = 13.06 grcm/volt.

For an open loop gain of 4000 the scaling is 100 volts at the output represents 2°

B is scaled at $13.06 \times \frac{4000}{5000}$ = 10.42 grcm/volt.

The example previously developed was for the NASA system. A similar procedure was followed on simulations for

the UA systems, such as UA-1, UA-2, and UA-6 systems. The UA-1 and UA-2 simulations were reported in Monthly Progress Report 3 and 4.

Since the UA-6 system represents the most recent attempt to optimize system performance, it will also be presented. To compare the transient response of the UA-6 system with previous system simulations, the system was simulated on the analog computer. The following discussion describes this simulation of the UA-6 system.

The forward loop simulation.

$$G(s) = \frac{13{,}000 \times 1.14\,(10^4)}{s(s^2 + 148^2)} \frac{\text{deg.}}{\text{gm cm}} = \frac{Y}{E} \qquad (16)$$

This is realized by the following computer circuit

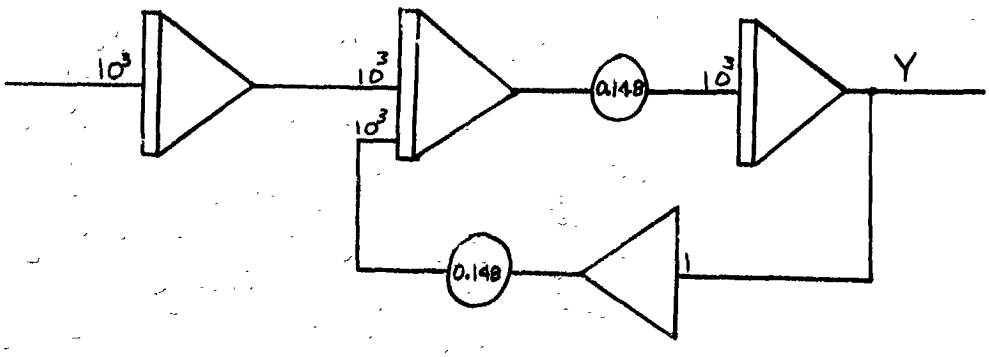


Figure 7. Circuit To Realize G(s)

therefore Y = 13,000 C.

$$H = K' \frac{s^4 + 340s^3 + 5.13(10^4)s^2 + 2.22(10^8)}{s^4 + 1501s^2 + 7.215(10^5)s^2 + 1.087(10^8)s + 1.08(10^8)} \quad (17)$$

For an open loop gain of 44, 340

$$K' = 4.15(10^4)$$

$$H = \frac{B}{C} = \frac{4.15(10^4)s^4 + 1.411(10^7)s^3 + 2.129(10^9)s^2 + 2.395(10^{11})s + 9.2(10)^{12}}{s^4 + 1.5(10^3)s^3 + 7.215(10^5)s^2 + 1.087(10^8)s + 1.08(10^8)} \quad (18)$$

$$\frac{B}{Y} = \frac{3.19s^4 + 1.085(10^3)s^3 + 1.63(10^5)s^2 + 1.842(10^7)s + 7.08(10^8)}{s^4 + 1.5(10^3)s^3 + 7.215(10^5)s^2 + 1.087(10^8)s + 1.08(10^8)} \quad (19)$$

$$B = \frac{1}{s^4}\left[7.08(10^8)Y - 1.08(10^8)B\right] + \frac{1}{s^3}\left[1.842(10^7)Y - 1.087(10^8)B\right]$$

$$+ \frac{1}{s^2}\left[1.63(10^5)Y - 7.215(10^5)B\right] + \frac{1}{s}\left[1.085(10^3)Y - 1.5(10^3)B\right]$$

$$+ 3.19Y \quad (20)$$

The feedback path can then be realized by the following computer

circuit.

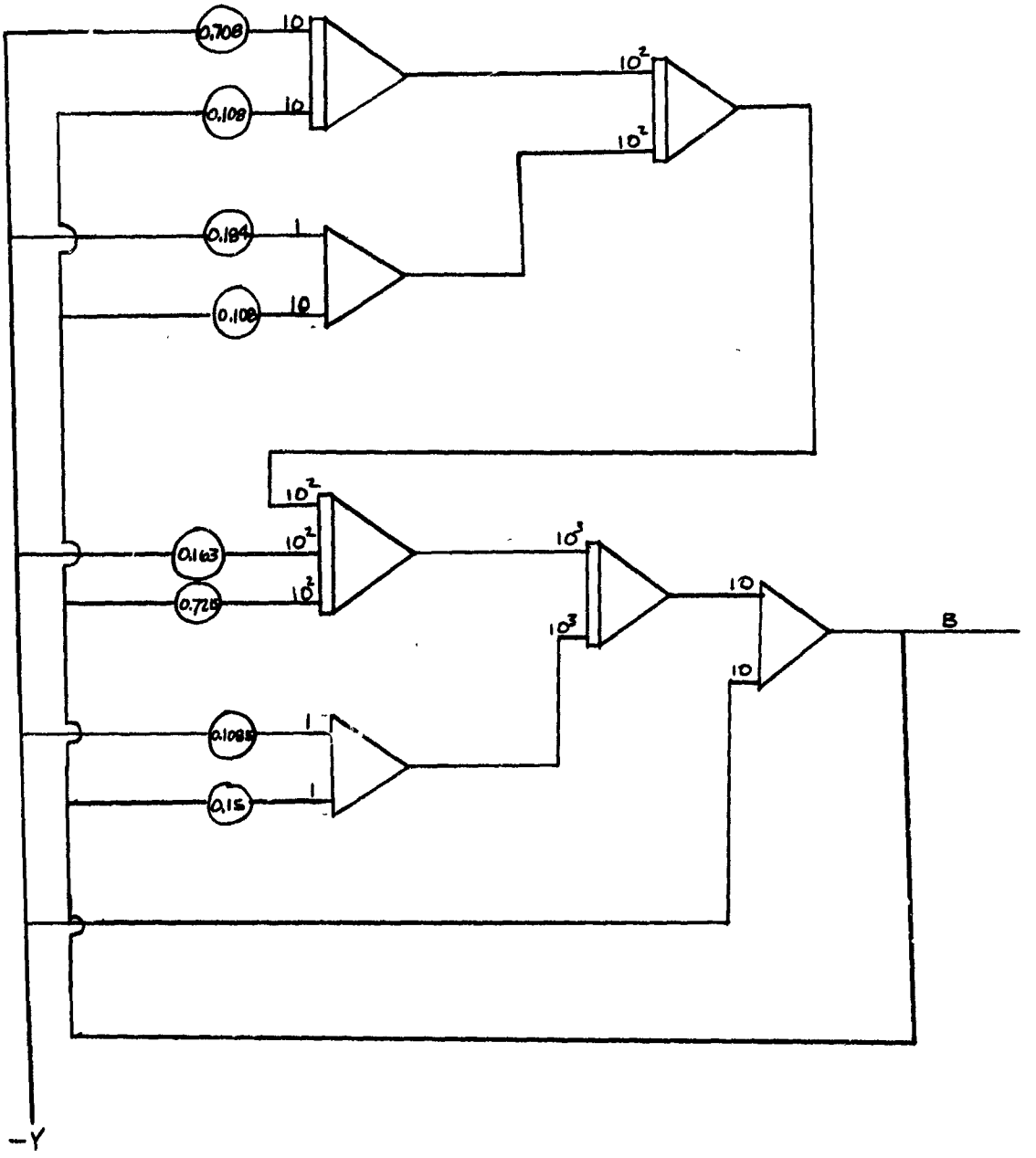


Figure 8. Circuit to Realize Feedback Path

Results of the simulation were interpreted as follows:

100 volts out of the forward loop was equated to 2°. The dc gain of the feedback simulation is 1.48 when the open loop gain is 10,000. For an open loop gain of 10,000, the actual feedback gain is 19,200 gm cm/degree.

Thus 1° represented by 50 volts gives 1.48 x 50 = 74 volts for B

But 1° x 19,200 gm cm/degree = 19,200 gm cm.

Thus 74 volts represents 19,200 gm cm or B is scaled at $\frac{19,200}{74}$ = 259.5 gm cm/volt.

For any open loop gain A, B is scaled at 259.5 x $\frac{A}{10,000}$ gm cm/volt.

The entire simulation was constructed as shown in Figure 9 where the pot marked A was used to vary the open loop gain.

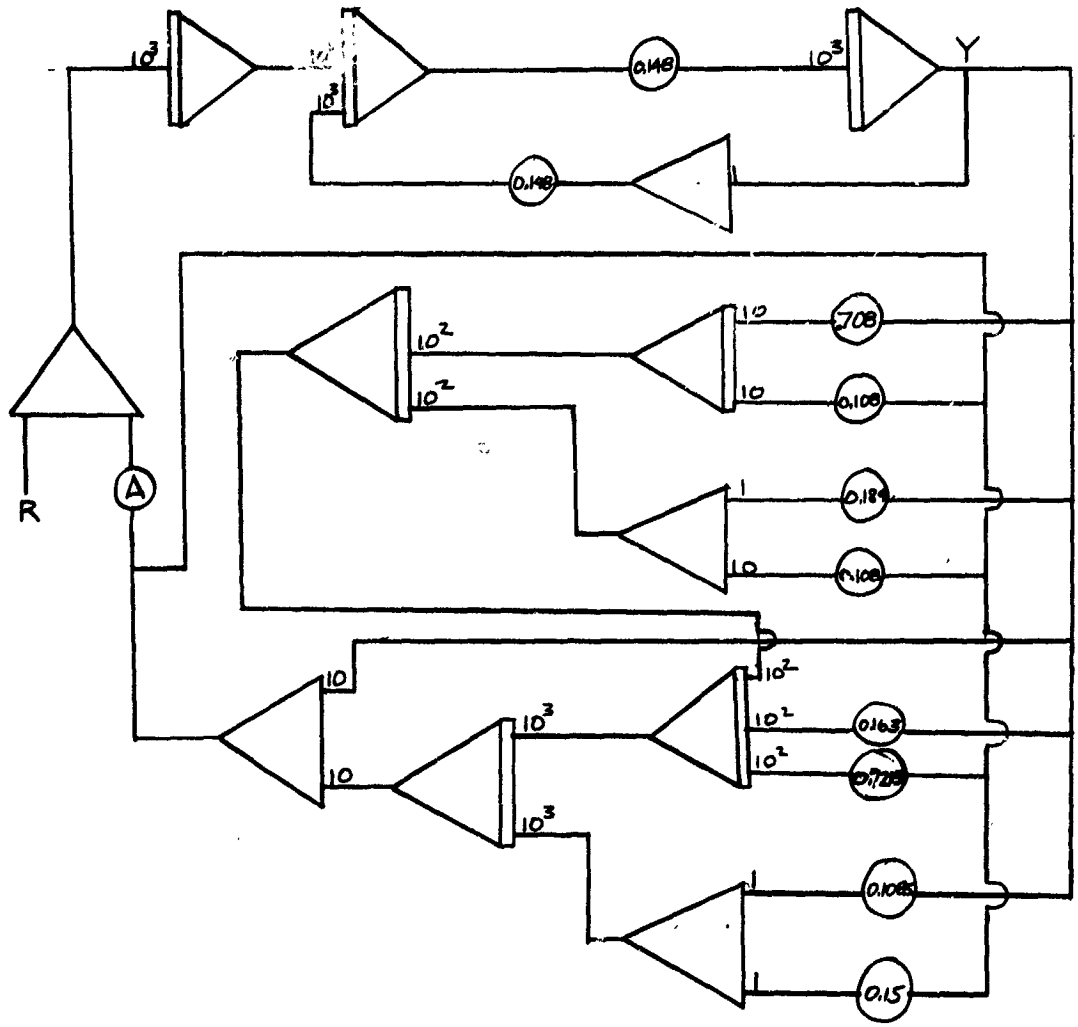


Figure 9. Circuit to Realize Entire Simulation.

3.0 PASSIVE NETWORK SYNTHESIS

Section 3.0 consists of four sections: 3.1.1 is concerned with the all passive R-C network synthesis of a 4-pole, 4-zero transfer function using network partitioning as an aid in the synthesizing process; 3.1.2 illustrates how a digital computer could be programmed to calculate the network parameters for the network developed in 3.1.1; 3.2 shows an R-C network synthesis technique for a two-pole, two-zero network; and 3.3 develops an R-C network synthesis pattern for a two-pole and a complex conjugate pair of zeros. All of the poles of the transfer function which is to be synthesized have poles on the negative real axis of the s plane in order that R-C networks can be used.

The synthesis tools developed in this report are by no means comprehensive, but indeed are rather specialized. As a result of an overall study, it was determined that the corrective transfer function would have a specified form such as

$$T_{12}(s) = K\frac{(s+\sigma_1)(s+\sigma_2)(\overline{s+\sigma_0}^2 + \omega_0^2)}{(s+\sigma_3)(s+\sigma_4)(s+\sigma_5)(s+\sigma_6)} \qquad (21)$$

where the inequalities

$$0 < \sigma_3 < 2\sigma_0 < \sigma_4 \quad \text{and} \quad 0 < \sigma_1 < \sigma_2 < \sigma_5 < \sigma_6$$

are satisfied. To use the formulas in the report, these inequalities must be satisfied. Other relations and other networks could be developed for transfer functions not meeting these restrictions, but it would take a considerable amount of time to develop simplified formulas for all possible pole-zero combinations.

3.1 All Passive Network

3.1.1 Synthesis with Network Partitioning

Frequently, considerable simplification may be made in the synthesis of a network to obtain a given transfer function by the use of network partitioning. A description of this method is given in several textbooks.[1,2]

The basis for partitioning is contained in the expression for the overall open-circuit voltage transfer function given in Equation 22 for two networks in cascade as shown in Figure 10. By dividing the numerator and denominator

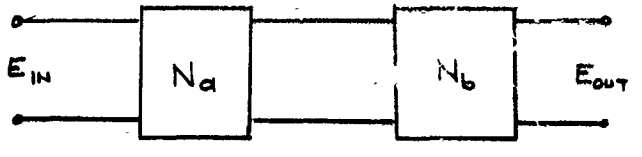


Figure 10. Partitioned Network

1. Babalanian, Network Synthesis, Prentice-Hall, pp. 314-318.
2. Truxal, Control System Synthesis, McGraw-Hill, pp. 218-220.

$$T_{12}(s) = \frac{E_{OUT}}{E_{IN}} = \frac{y_{12a}\, y_{12b}}{y_{11b} + y_{22a}} \qquad (22)$$

of Equation 22 by an appropriate polynomial and assigning appropriate roots of the polynomial to y_{12a} and y_{12b}, it is possible to determine the four admittances given in Equation 22.

As an example, consider the open-circuit voltage ratio given in Equation 23. It is desired to obtain an RC network terminated in a resistor which will have the voltage

$$T_{12}(s) = K\frac{(s+82)(s+184)\left[(s+50)^2+(130)^2\right]}{(s+2)(s+300)(s+1000)(s+1200)} \qquad (23)$$

gain given in Equation 23.

Since the network is to have only resistance and capacitance, the driving point admittances must have alternating poles and zeros on the negative real axis with a zero as the lowest critical frequency. Thus the polynomial used to divide the denominator and the numerator of Equation 23 must be of third or fourth degree. In the interest of simplicity, a third degree polynomial will be chosen here. Thus

the division of the denominator results in Equation 24 where the restriction on the poles of the driving point admittances are given in Equation 25.

$$y_{11b} + y_{22a} = \frac{(s+2)(s+300)(s+1000)(s+1200)}{(s+\sigma_1)(s+\sigma_2)(s+\sigma_3)} \tag{24}$$

$$2 < \sigma_1 < 300 < \sigma_2 < 1000 < \sigma_3 < 1200 \tag{25}$$

To insure that the network N_b will be terminated in a resistor, it is necessary that $-y_{12b}$ does not have a pole at infinity. Thus any two of the poles may be assigned to the network N_b. Arbitrarily choosing σ_2 and σ_3 as the poles for network N_b results in the expressions for the transfer admittances given in Equation 26 and Equation 27.

$$-y_{12a} = K_a \frac{(s+50)^2 + (130)^2}{s+\sigma_1} \tag{26}$$

$$-y_{12b} = K_b \frac{(s+82)(s+184)}{(s+\sigma_2)(s+\sigma_3)} \tag{27}$$

The values for σ_1, σ_2, and σ_3 are now chosen in order

that Equation 24 may be expanded by partial fractions and y_{11b} and y_{22a} can be determined. A suitable set of values consistent with the constraints given by Equation 25 is shown below.

$$\sigma_1 = 100 \qquad \sigma_2 = 500 \qquad \sigma_3 = 1100$$

The partial fraction expansion of Equation 24 is given in Equation 28.

$$y_{11b} + y_{22a} = 13.09 + s + \frac{485.1s}{s+100} + \frac{290.5s}{s+500} + \frac{13.31s}{s+1100} \quad (28)$$

Part of the constant term in Equation 28 is arbitrarily assigned to y_{11b} and the remainder to y_{22a}. The other terms must be assigned so that y_{11b} has the same poles as y_{12b} and so that y_{22a} has the same poles as y_{12a}. A suitable assignment is given in Equation 29 and Equation 30.

$$y_{22a} = 7 + s + \frac{485.1s}{s+100} = \frac{s^2 + 592.1s + 700}{s+100} \quad (29)$$

$$y_{11b} = 6.09 + \frac{290.5s}{s+500} + \frac{13.31s}{s+1100} = \frac{309.9s^2 + 3.35(10^5)s + 3.35(10^4)}{(s+500)(s+1100)} \quad (30)$$

Substituting the assigned values for the σ's in Equation 24 and 27 gives Equations 31 and 32.

$$-y_{12a} = K_a \frac{(s+50)^2 + (130)^2}{s+100} \tag{31}$$

$$-y_{12b} = K_b \frac{(s+82)(s+184)}{(s+500)(s+1100)} \tag{32}$$

Equations 29 through 32 give the transfer and driving point admittances for each of the cascaded networds N_a and N_b. Each network may now be determined separately.

Determination of Network N_b. The expressions for the transfer and driving point admittances are given in Equations 30 and 32 and are repeated here in factored form.

$$y_{11b} = 309.9 \frac{(s+10.06)(s+1074)}{(s+500)(s+1100)} \tag{33}$$

$$-y_{12b} = K_b \frac{(s+82)(s+184)}{(s+500)(s+1100)} \tag{34}$$

This network may be realized in the form of a ladder by the process of repeated zero shifting and pole removal. Table 1, which summarizes the operations performed, is given on the following page. The numerical cal-

culations are as follows.

$$y_2(s) = y_{11b}(s) - \frac{A s}{s+500}$$

$$A = \frac{s+500}{s}\, y_{11b}(s)\Big|_{s=-82} = 264.9$$

$$y_{11b} - y_2 = \frac{264.9\, s}{s+500} = \frac{1}{0.003775 + \frac{1}{0.52986}}$$

$$y_2 = 44.98\ \frac{(s+82)(s+908.2)}{(s+500)(s+1100)}$$

$$z_2 = \frac{1}{y_2} = 0.02223\ \frac{(s+500)(s+1100)}{(s+82)(s+908.2)}$$

$$z_3 = z_2 - \frac{K_1}{(s+82)}$$

$$K_1 = (s+82)\, z_2\Big|_{s=-82} = 11.45$$

$$z_2 - z_3 = \frac{1}{0.08738\, s + \frac{1}{0.1396}}$$

$$z_3 = 0.02223\ \frac{s+1003}{s+908.2}$$

$$y_3 = \frac{1}{z_3} = 44.98\ \frac{s+908.2}{s+1003}$$

$$y_4 = y_3(s) - y_3(-184) = y_3(s) - 39.78 = y - \frac{1}{0.02514} = 52.06\,\frac{s+184}{s+1003}$$

$$z_4 = 0.1921\ \frac{s+1003}{s+184}$$

$$z_5 = z_4 - \frac{K_2}{s+184}$$

$$K_2 = (s+184)\, z_5\Big|_{s=-184} = 15.73$$

$$z_4 - z_5 = \frac{1}{0.06356\, s + \frac{1}{0.08550}}$$

$$z_5 = 0.01921 = \frac{1}{y_5}$$

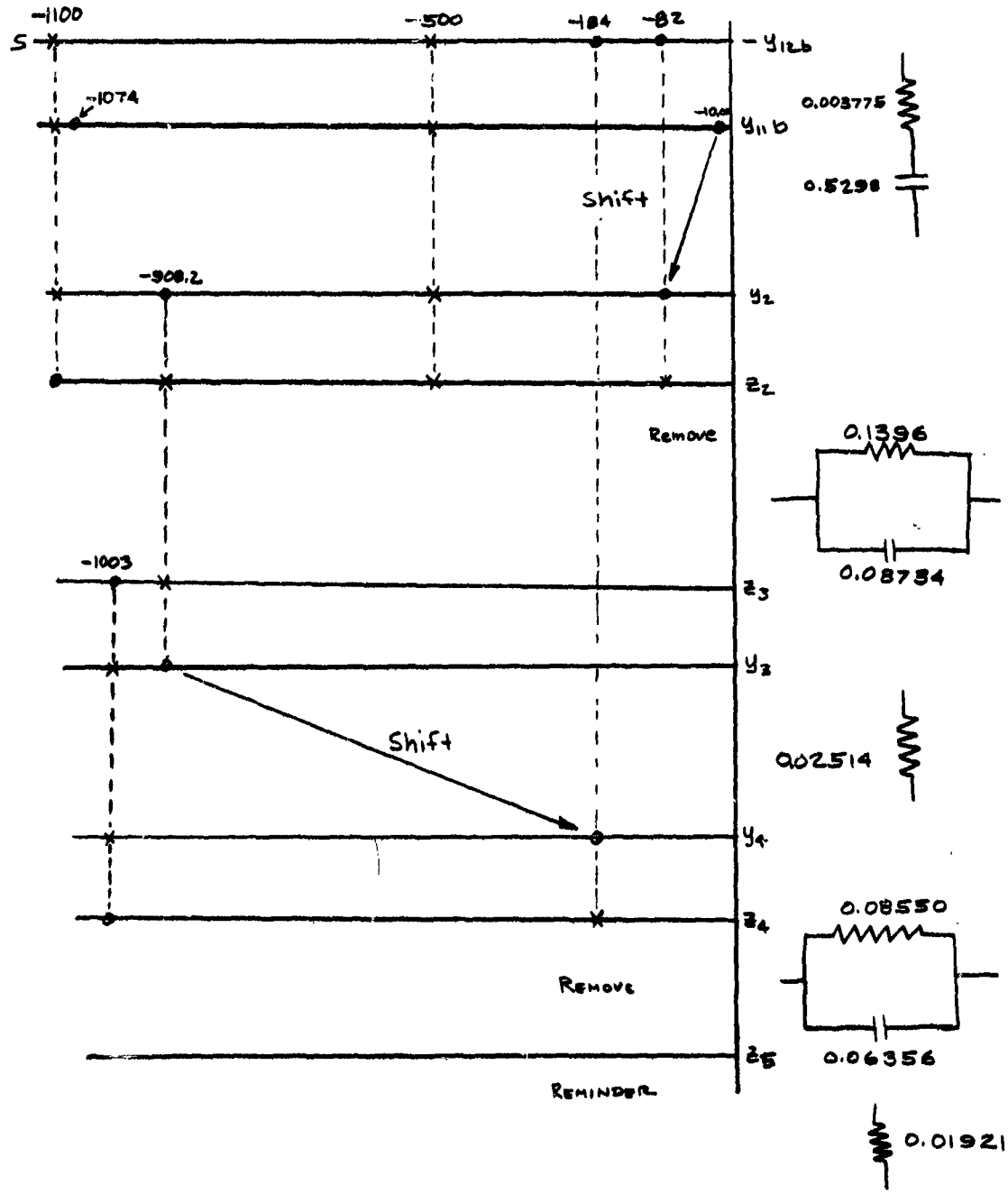


Table 1 - Summary of Shifting and Removal Operations

Network N_b is shown in Figure 11.

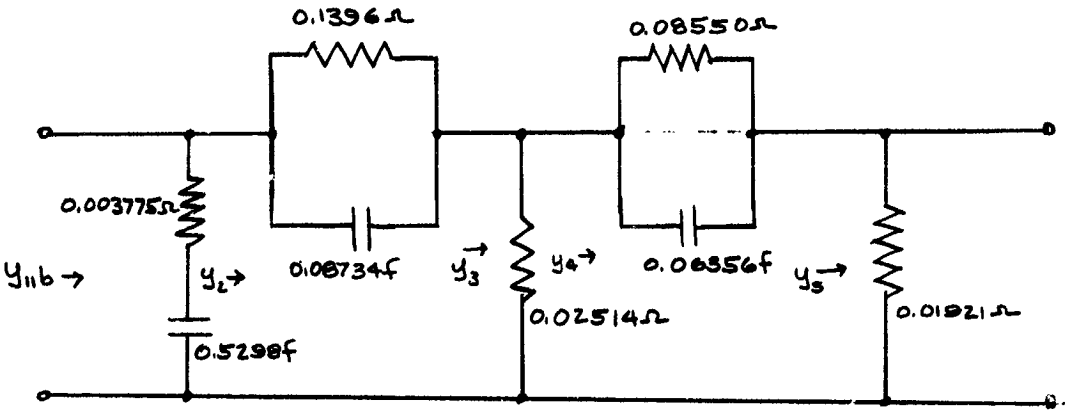


Figure 11. Network N_b

Determination of Network N_a. The expressions given by Equations 35 and 36 for the driving point and transfer admittances are repeated here.

$$y_{22a} = \frac{s^2+592.1s+700}{s+100} \tag{35}$$

$$-y_{12a} = K_a \frac{(s+50)^2+130^2}{s+100} = K_a \frac{s^2+100s+19400}{s+100} \tag{36}$$

The Dasher Method may be used here to realize the network. First, a shunt element is removed from the output so that the constant term in the numerator of the driving

point function becomes equal to the constant term in the numerator of the transfer function. Either a resistance or a capacitance may be used, depending on the relative numerical values involved. Here a capacitance is used since 700 is less than 19,400.

$$y'_{22a} = y_{22a} - sC = (1-C)\ \frac{s^2 + \left(\frac{592.1 - 100C}{1-C}\right)s + \frac{700}{1-C}}{s+100}$$

$$\frac{700}{1-C} = 19{,}400 \qquad C = 0.964$$

$$y'_{22a} = 0.036\ \frac{s^2 + 13{,}740s + 19{,}400}{s+100}$$

Expanding by partial fractions yields the following expression.

$$y'_{22a} = 0.036\left[s + 194 + \frac{13{,}440s}{s+100}\right]$$

The expression for y_{22a} is now in the form used in one of the references.[3] Using the notation of this reference yields the following expressions.

3. Babanian, Network Synthesis, Prentice-Hall. pp. 298-299.

$\sigma_c = 100$

$K = 0.036$

$K_{\infty} = 194$

$K_{12} = 194$

$\sigma_0 = 50$

$\frac{K_{12}}{a} = 13440$

Thus $a = \frac{194}{13,440} = 0.01443$

Using Figure 7 - 33(a) of the reference[4]

$C_1 = K = 0.036$

$G_1 = K K_{oc}(a+1) = 7.101 = \frac{1}{0.1408}$

$C_2 = \frac{K K_{12}(a+1)^2}{a\,\sigma_c} = 4.992$

$G_2 = \infty$

$\frac{G_1}{a} = 492.1 = \frac{1}{0.00203}$

Thus the circuit for realizing the network N_a becomes that shown in Figure 12.

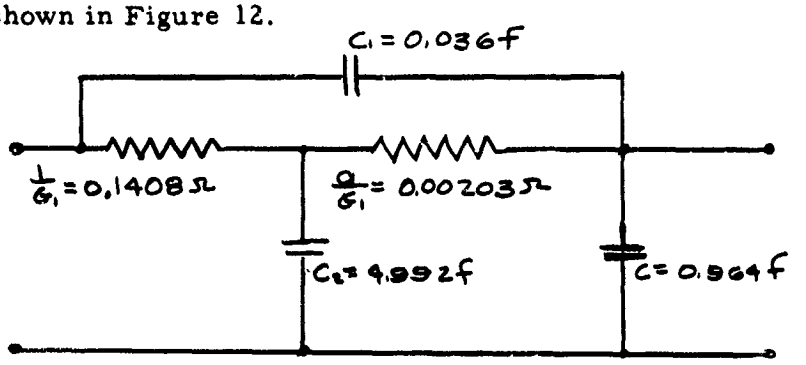


Figure 12. Network N_a

4. Ibid. p. 306.

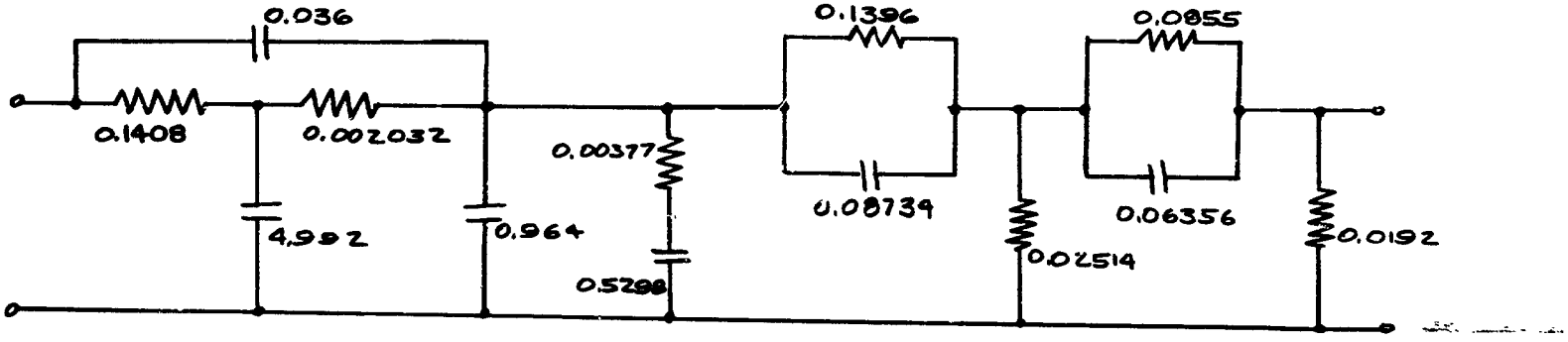


Fig. 13 Composite Network - Values in farads and ohms

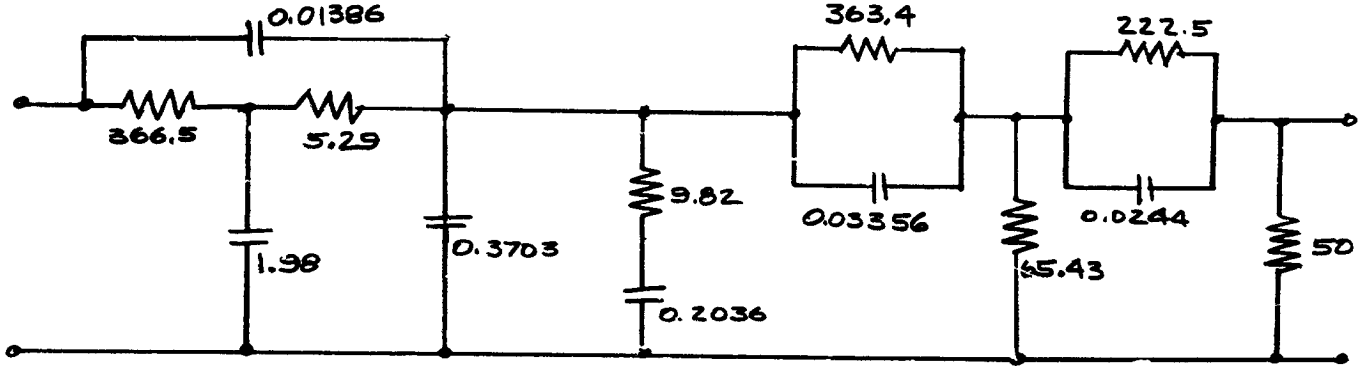


Fig. 14 Scaled Network - Values in μf and kilo ohms.

The entire network is found by cascading the networks of Figure 11 and 12 and is given in Figure 13.

If it is desired to terminate the network in a 50K resistor, the values of the elements may be scaled to yield the network of Figure 14. Analysis of the circuit of Figure 14 shows the d-c gain to be

$$T_{12}(0) = 0.01228 \quad .$$

3.1.2 Digital Computer Solution to Determine Networks

It was hoped that a successful digital computer program could be completed to facilitate R-C ladder synthesis procedures. At this time the program performs adequately in part, but not as a continuous program. Never the less, the use of a digital computer would simplify the problem solution considerably and the following explanation describes a procedure that could be followed.

The network partitioning procedure follows the discussion of Section 3.1.1, which illustrates how to realize complex zero's using only R-C elements.

$$\frac{E_o}{E_i} = K \frac{\left[(s+a_1)^2 + a_2^2\right](s+b_1)(s+b_2)}{(s+c_1)(s+c_2)(s+c_3)(s+c_4)} = \frac{y_{12a}\, y_{12b}}{y_{11b} + y_{22a}}$$

$$b_1 < b_2 \qquad c_1 < c_2 < c_3 < c_4$$

$$y_{11b} + y_{22a} = \frac{(s+c_1)(s+c_2)(s+c_3)(s+c_4)}{(s+\sigma_1)(s+\sigma_2)(s+\sigma_3)}$$

$$= s + k_0 + \frac{k_1 s}{s+\sigma_1} + \frac{k_2 s}{s+\sigma_2} + \frac{k}{s}$$

$$c_1 < \sigma_1 < c_2 < \sigma_2 < c_3 < \sigma_3 < c_4$$

$$-y_{12a} = k_a \frac{(s+a_1)^2 + a_2^2}{s+c_3} \tag{37}$$

$$-y_{12b} = k_b \frac{(s+b_1)(s+b_2)}{(s+\sigma_1)(s+\sigma_2)} \tag{38}$$

$$y_{11b} = k_0 \phi' + \frac{k_1 s}{s+\sigma_1} + \frac{k_2 s}{s+\sigma_2} \tag{39}$$

$$y_{22a} = s + k_0 (1-\phi) + \frac{k_3 s}{s+\sigma_3} \tag{40}$$

$$0 \leq \phi \leq 1$$

For the circuit shown in Figure 15, Equations 37 and 40 describe the (a) network while Equations 38 and 39 describe the (b) network.

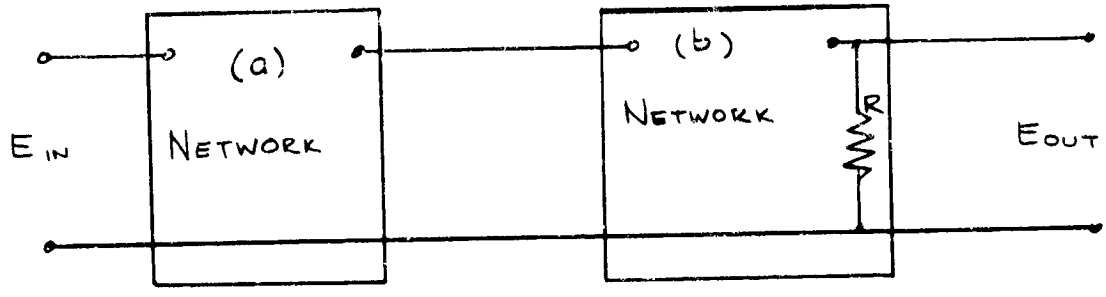


Figure 15. A Partitioned Network.

Furthermore, network (a) can be realized by combining two ladders in parallel. This could then realize the complex pair of zeros. The (a) network would then be equivalent to networks (I) and (II) connected as shown in Figure 16.

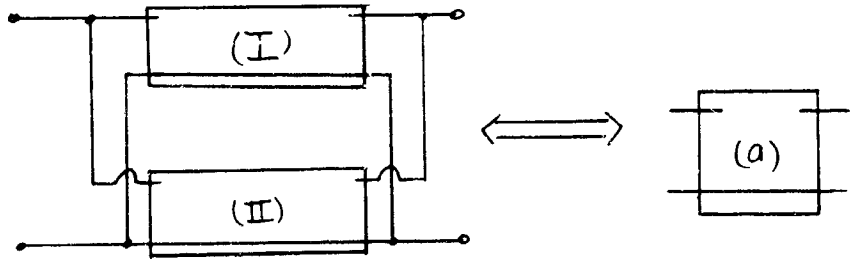


Figure 16. Use of Parallel Ladders to Realize Network (a).

The equations describing networks (I) and (II) can then be obtained as follows:

$$-y_{12a} = K_a \frac{s^2 + 2a_1 s + (a_1^2 + a_2^2)}{s + \sigma_3}$$

$$y_{22a} = s + k_0 \left(1 - \frac{s}{q}\right) + \frac{k_3}{s + \sigma_3}$$

$$\left.\begin{aligned} -y_{12}^{I} &= K' \frac{s(s+\epsilon)}{s+\sigma_3} \\ -y_{12}^{II} &= K'' \frac{s + \frac{a_1^2 + a_2^2}{2a_1 - \epsilon}}{s + \sigma_3} \end{aligned}\right\} \quad 0 < \epsilon < 2a_1$$

After determining each ladder, compute K' and K''. Then adjust the admittance levels of each ladder as follows:

$$\frac{1}{K_a} = \frac{1}{K'} + \frac{2a_1 - \epsilon}{K''}$$

Multiply the admittance level of network (I) by:

$$\frac{K_a}{K'}$$

and multiply the admittance level of network II by

$$\frac{2q_1 - \epsilon}{K''} K_q$$

Finally, the impedance levels of all networks are changed to give the proper value of the resistance R (load resistance) shown in Figure 15.

The digital program to partition the network as shown above would operate in a manner similar to the one shown by the flow chart in Figure 17.

This constitutes the first part of the program and provides the equations needed to synthesize networks (I), (II), and (b). Probably, this first part could as easily be done on a desk calculator since the next step must be done by hand anyway.

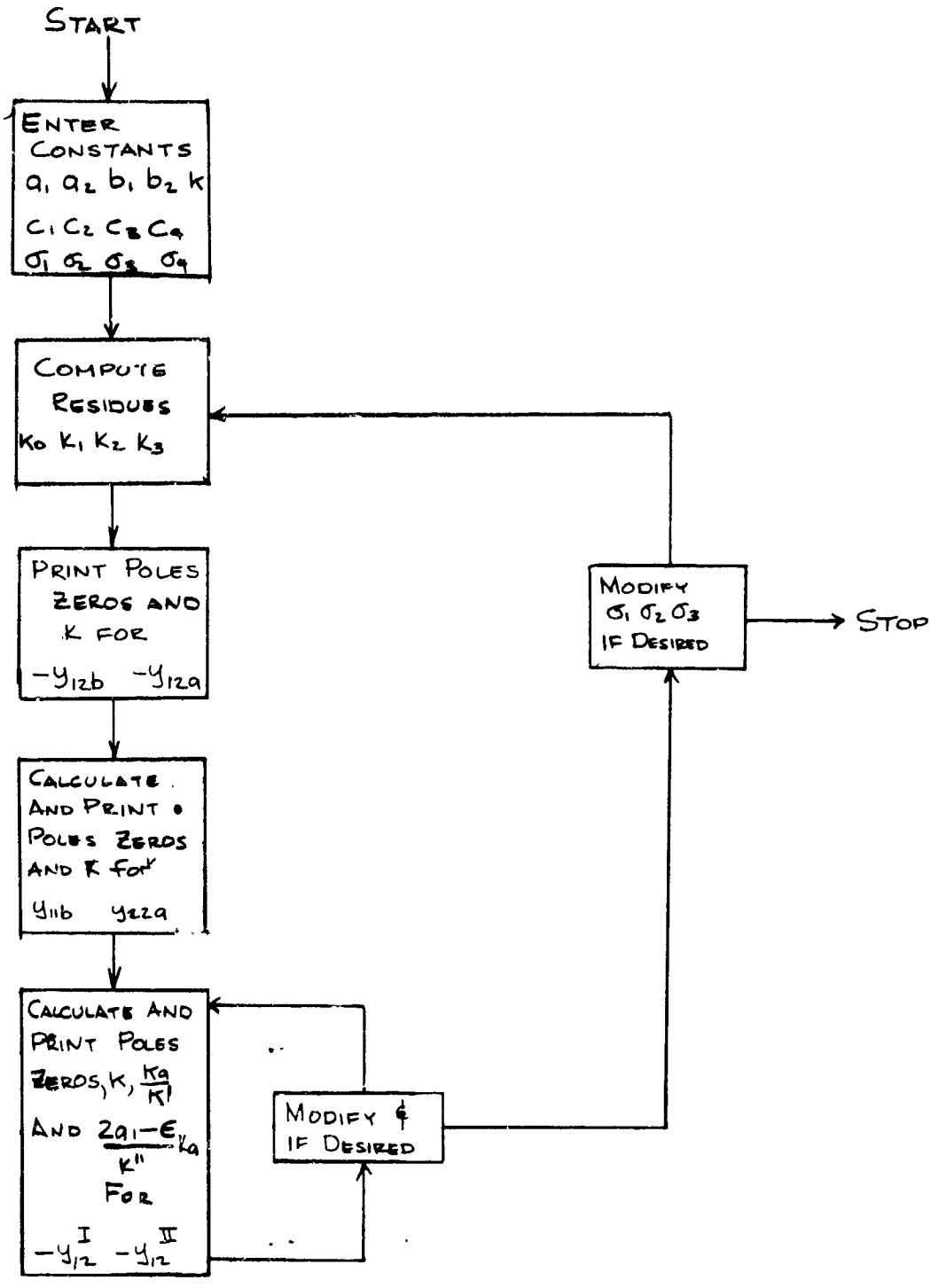


Figure 17. Flow Chart for Network Partitioning

The next part of the process requires plotting the poles and zeros of $-y_{12}$ and y_{22} as functions of (s) as shown for some fictitious problem in Figure 18. By inspection of these pole-zero plots, the steps of shifting zeros and removing poles can be listed. Since the locations of the transmission zeros are specified, we know where to shift the zeros of y_{22} and of course the locations where pole removals will be made. The following operations are permitted:

(1) Shifting
   (a) removal of a constant from Z or Y
   (b) partial pole removal from Z or Y

(2) Removal - Total pole removal from Z or Y.

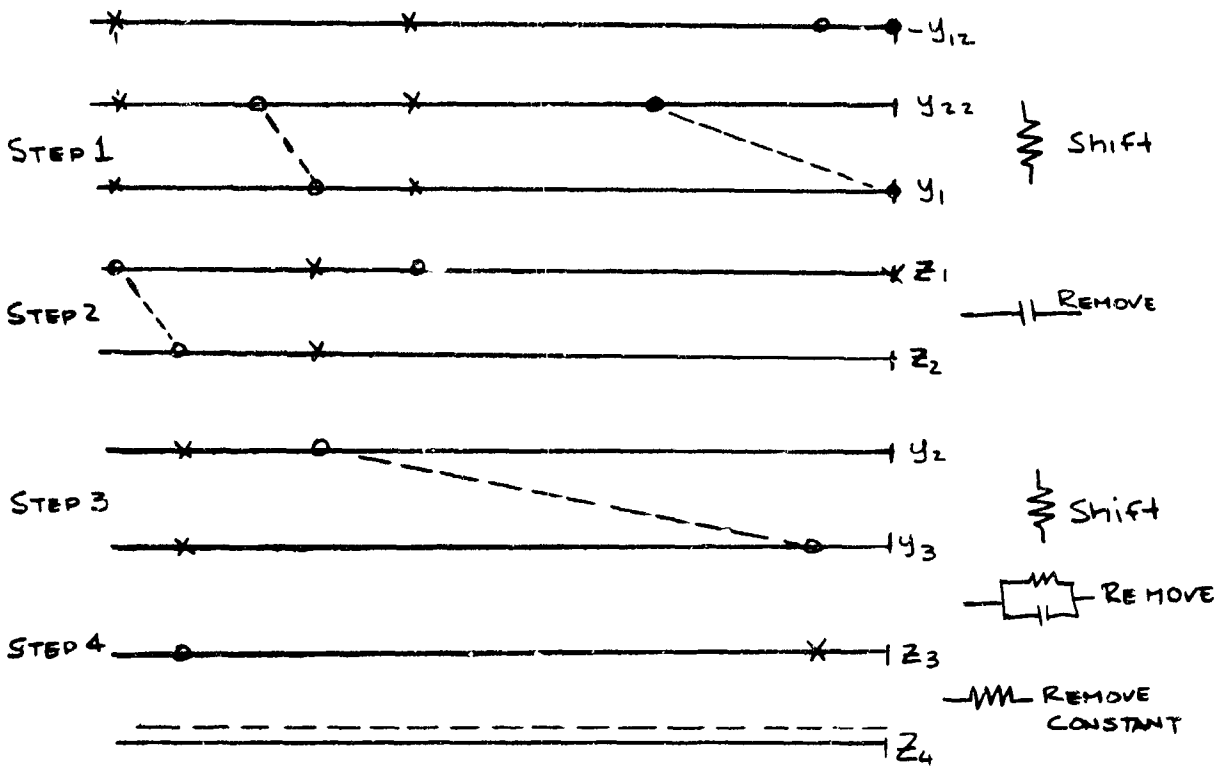


Figure 18. Example Pole-Zero Pattern and Realization Procedures.

Knowing then in what order the steps are to be taken and what we need to do at each step, we can again program the computer to make the calculations for us.

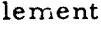
The computer program for this part contains six subroutines for shifting and pole removal. These subroutines and operating procedures are as follows:

Shifting by removal of a constant impedance

Operation: Creates a zero of transmission in the driving point impedance at $s = -\alpha$

Procedure: $Z_{i+1}(s) = Z_i(s) - Z(-\alpha)$

Therefore $Z_{i+1}(s)\Big|_{s=-\alpha} = 0$

Element removed:  $R = Z(-\alpha)$

Shifting by removal of a constant admittance

Operation: Creates a zero of transmission in the driving point admittance at $s = -\alpha$

Procedure: $Y_{i+1}(s) = Y_i(s) - Y(-\alpha)$

therefore $Y_{i+1}(s)\Big|_{s=-\alpha} = 0$

Element removed:  $R = Z(-\alpha)$

Shifting by removing part of a pole of the impedance function

Operation: Creates a zero of transmission in the driving point impedance at $s = (-\alpha)$ by removing part of the pole at $s = (-\beta)$ where $\beta < -\beta \leq A$. Since the location of the pole at $s = (-\beta)$ is not known exactly, the computer finds the root satisfying $\beta \leq -\beta \leq A$ where A and B can be guessed at from the pole-zero plot as a function of s.

Procedure: $$Z_{i+1}(s) = Z_i(s) - \frac{\beta-\alpha}{s+\beta} Z(-\alpha)$$

therefore $Z_{i+1}(s)\Big|_{s=-\alpha} = 0$

Elements removed:  $R = \frac{\beta-\alpha}{\beta} Z(-\alpha)$

$C = \frac{1}{R\beta}$

Shifting by removing part of a pole of the admittance function

Operation: Same as the partial pole removal described except that a zero is created in the driving point admittance.

Procedure: $$Y_{i+1}(s) = Y_i(s) - \frac{\alpha - \beta}{\alpha Z(-\alpha)} \frac{s}{s+\beta}$$

therefore $$Y_{i+1}(s)\Big|_{s=-\alpha} = 0$$

Elements removed:

$$R = \frac{\alpha Z(-\alpha)}{\alpha - \beta}$$

$$C = \frac{1}{R\beta}$$

Transmission zero realization from the admittance function

Operation Realizes a transmission zero at $s = (-\gamma)$ where $Y(-\gamma) = 0$

Procedure: $$Z_{i+1}(s) = Z_i(s) - \frac{\left[(s+\gamma) Z(s)\right]_{s=-\gamma}}{s+\gamma}$$

Elements removed: $$R = \frac{1}{\gamma}\left[(s+\gamma) Z(s)\right]_{s=-\gamma}$$

$$C = \frac{1}{R\gamma}$$

Transmission zero realization from the

impedance function

Operation: Realizes a transmission zero at $s = (-\gamma)$ where $Y(-\gamma) = 0$

Procedure: $$Y_{i+1}(s) = Y_i(s) - \frac{s}{s+\gamma}\left[\frac{(s+\gamma)Y(s)}{s}\right]_{s=-\gamma}$$

Elements removed

$$R = \frac{s}{(s+\gamma)Y(s)}\Big|_{s=-\gamma}$$

$$C = \frac{1}{R\gamma}$$

The program performing this part of the procedure was flow-charted in Figure 19.

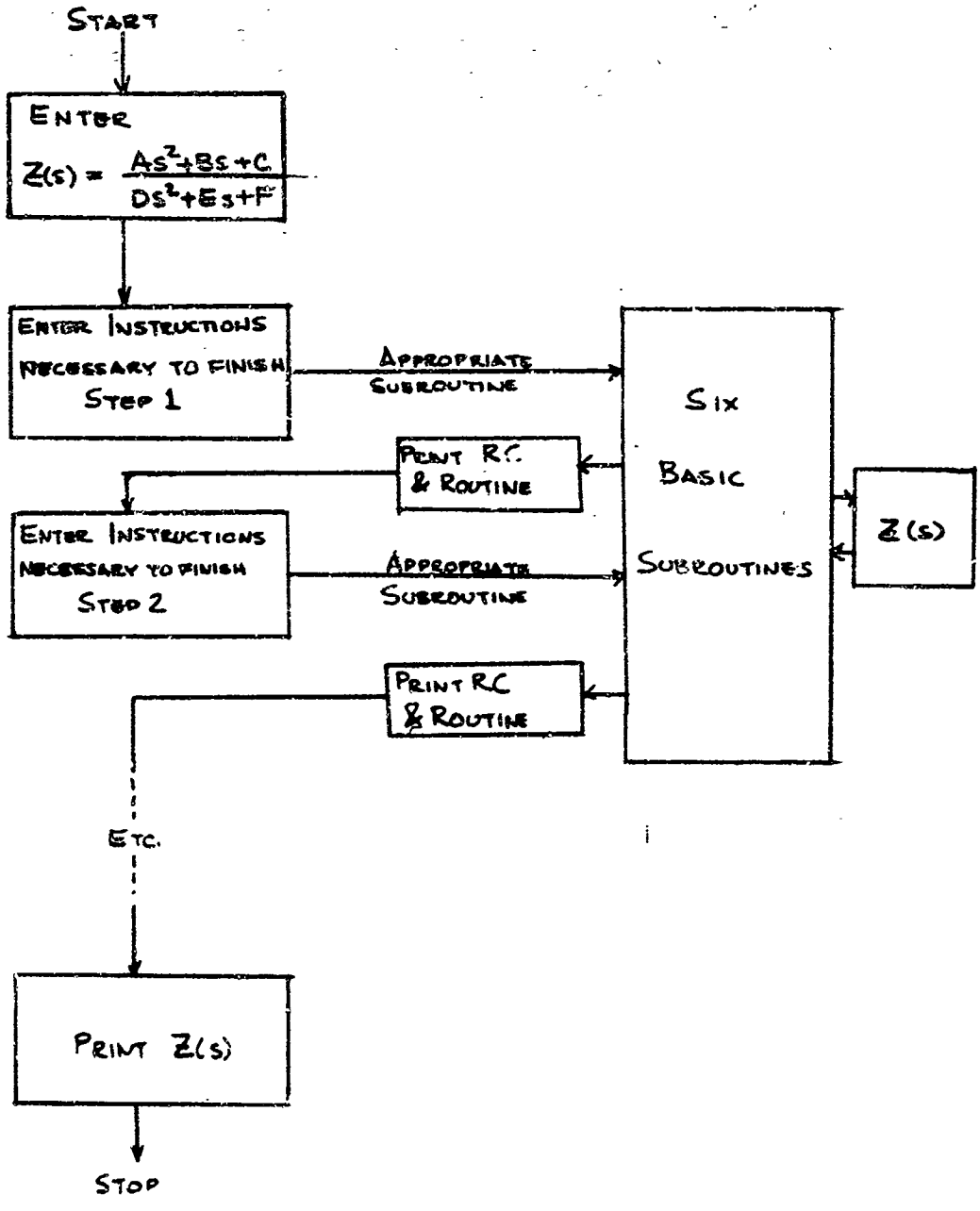


Figure 19. Flow Chart for Ladder Realization

Obviously, some subroutine operation may fail if $Z(s)$ fails to be positive real of if the limits A and B are incorrectly guessed. The program should then indicate the nature of the error so that an appropriate correction may be made.

The computer program for the flow chart shown in Figure 19 has proven itself and is relatively simple in nature. The program for partitioning the network is more laborious to construct and has proven useful only in generating the equations for network (b). The derivation of the equations for networks (I) and (II) could also be programmed.

Since this program was not run in a compatible language, it is not included in this report.

3.2 R-C Network Synthesis for Real Poles and Zeros

A number of techniques are available for synthesis of open-circuit voltages transfer functions with R-C networks. One common method used results in a ladder network. Even here a variety of networks may be obtained, depending not only on the relative values of the poles and zeros of the transfer functions, but also on the arbitrary choices made in manner and order of realizing the zeros of the network. Hence, it is not feasible to provide all the possible network configurations for a transfer function having only two real poles and two real zeros. The methods used are outlined in most standard textbooks on the subject.[1]

An example will be given here for an open-circuit transfer function as given in Equation 41 in which both zeros are smaller than the poles as provided by Equation 42.

$$T_{12}(s) = K \frac{(s+a)(s+b)}{(s+c)(s+d)} \tag{41}$$

$$0 < a < b < c < d \tag{42}$$

*1. Truxal, Control System Synthesis, McGraw-Hill, pp. 187-202. Van Valkenburg, Introduction to Modern Network Synthesis, John Wiley and Sons, pp. 270-288.

The first step requires recognition of the relation between the open-circuit voltage transfer function and the short-circuit admittances as given in Equation 43. Then it must be recognized that y_{12} and y_{22}

$$\overline{T}_{12}(s) = -\frac{y_{12}}{y_{22}} \tag{43}$$

have the same poles. In this case, a single pole is sufficient as shown in Equations 44 and 45. This pole must be chosen to make y_{22} an R-C function and is restricted by the relation of Equation 46.

$$-y_{12} = K\frac{(s+a)(s+b)}{(s+\sigma)} \tag{44}$$

$$y_{22} = \frac{(s+c)(s+d)}{(s+\sigma)} \tag{45}$$

$$c < \sigma < d \tag{46}$$

The synthesis proceeds by an alternate removal of elements to shift the zeros of the driving point admittance and to realize these zeros by pole removal in this example. Figure 20 shows a plot of the various steps with the various driving

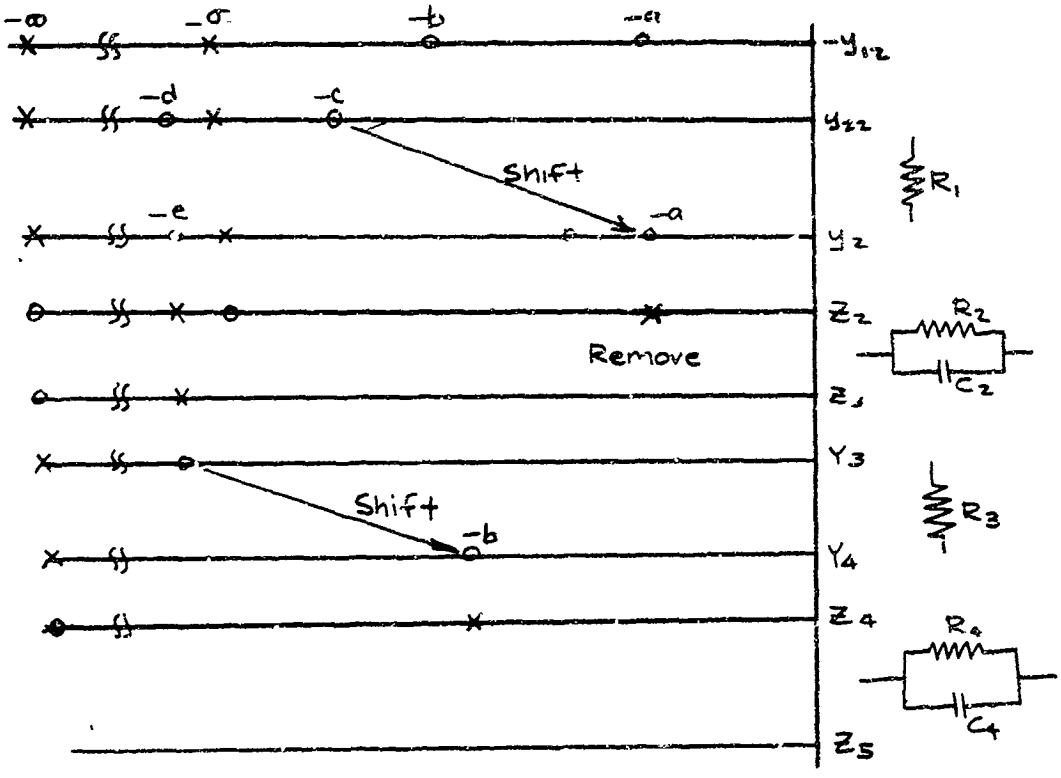


Figure 20. Realization of Poles and Zeros

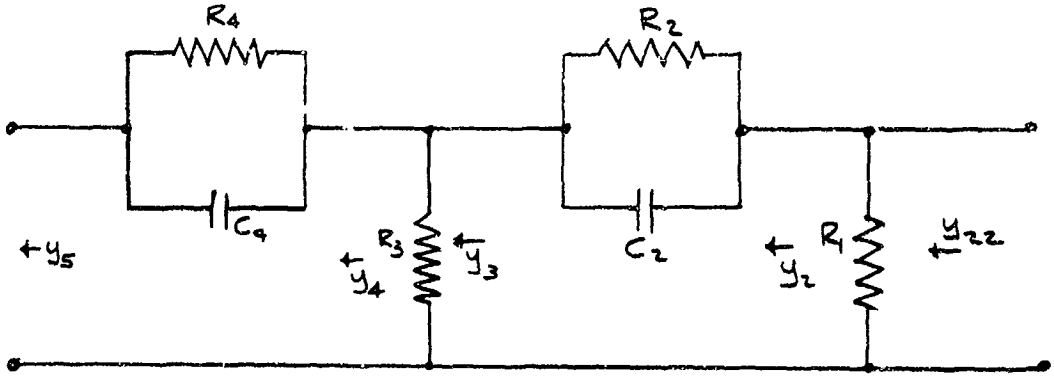


Figure 21. Circuit Realizing Poles and Zeros

point impedances and admittances identified in Figure 21. The elements realized at each step are shown on the right hand side of the table.

The values of the elements in Figure 21 are given by Equations 47 through 52 and the value of e is given in Equation 53.

$$R_1 = \frac{(\sigma - a)}{(c-a)(d-a)} \tag{47}$$

$$R_2 = \frac{(\sigma - a)}{a(e-a)} \tag{48}$$

$$R_3 = \frac{(e-\sigma)}{(e-b)(e-a)} \tag{49}$$

$$R_4 = \frac{(e-\sigma)}{b(e-a)} \tag{50}$$

$$C_2 = \frac{(e-a)}{(\sigma-a)} \tag{51}$$

$$C_4 = \frac{(e-a)}{(e-\sigma)} \tag{52}$$

$$e = \frac{\sigma(c-a) + d(\sigma-c)}{(\sigma-a)} \tag{53}$$

Frequently it is desirable to consider the resistance R_1 as the load impedance and scale the impedance in the network so that this resistance has some specific value. The results of each scaling are given in Figure 22 and the values of the elements given in Equations 54 through 55. Here the values of e as given by Equation 53 has been incorporated in the values.

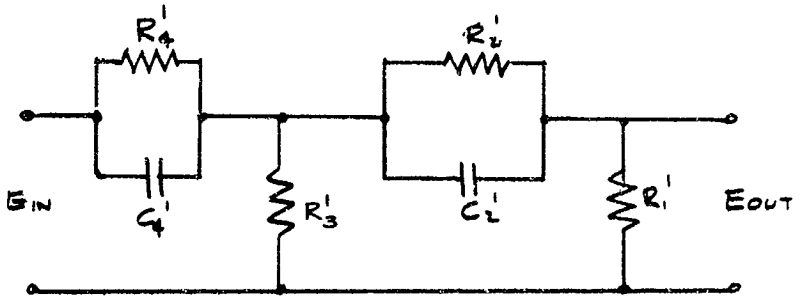


Figure 22. Circuit after scaling.

$$R'_2 = \frac{(c-a)(d-a)(\sigma-a)\ R'_1}{a\left[\sigma(c-a)+d(\sigma-c)-a(\sigma-a)\right]} \qquad (54)$$

$$R'_3 = \frac{(c-a)(d-a)(\sigma-c)(d-\sigma)\ R'_1}{\left[\sigma(c-a)+d(\sigma-c)-b(\sigma-a)\right]\left[\sigma(c-a)+d(\sigma-c)-a(\sigma-a)\right]} \qquad (55)$$

$$R'_4 = \frac{(c-a)(d-a)(\sigma-c)(d-\sigma)\ R'_1}{b(\sigma-a)\left[\sigma(c-a)+d(\sigma-c)-a(\sigma-a)\right]} \qquad (56)$$

$$C'_2 = \frac{\sigma(c-a)+d(\sigma-c)-a(\sigma-a)}{(c-a)(d-a)(\sigma-a)\ R'_1} \qquad (57)$$

$$C_4' = \frac{(\sigma-a)[\sigma(c-a)+d(\sigma-c)-a(\sigma-a)]}{(c-a)(d-a)(\sigma-c)(d-\sigma)R_1'} \qquad (58)$$

The d-c open circuit voltage gain is given in Equation 59.

$$T_{12}(o) = \frac{ab}{cd} \qquad (59)$$

Although the choice of σ is arbitrary within the limits given in Equation 6, a value should be chosen about midway between c and d to prevent the capacitance C_4' from becoming excessively large.

3.3 R-C Network Synthesis for Real Poles and Complex Zeros

Only the second order voltage transfer function

$$T_{12}(s) = K_1 \frac{(s+\sigma_o)^2+\omega_o^2}{(s+\sigma_1)(s+\sigma_2)} = \frac{E_{OUT}}{E_{IN}} \qquad (60)$$

will be considered here, where K_1, ω_o, σ_o, σ_1 and σ_2 are real, positive numbers.

While there are several methods for determining a

network having the transfer function given by Equation 60, the results presented here are only for the Dasher realization. One such realization is shown in Figure 23 which is valid provided that the poles conform to Equation 61.

$$\sigma_1 < 2\sigma_0 < \sigma_2 \tag{61}$$

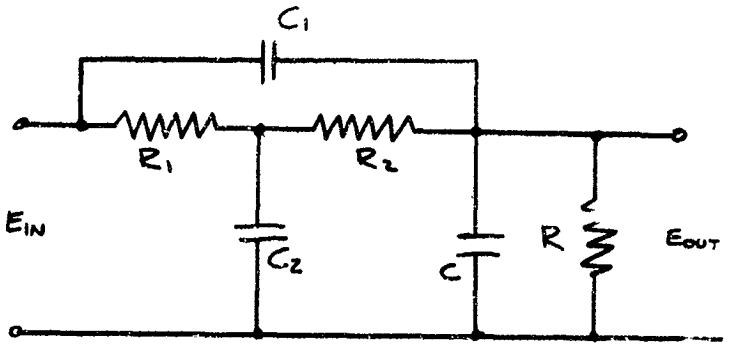


Figure 23. R-C Network with Complex Zeros in Transfer Function.

The network of Figure 23 will have the open-circuit voltage transfer ratio given in Equation 60. Thus the impedance of any load attached to the network must be included in the resistance R and capacitance C.

The values of the components in Figure 23 are given by the following equations:

$$C_1 = \frac{\sigma_1\sigma_2 - 2\sigma_0\gamma}{(\sigma_0^2 + \omega_0^2)\gamma R} \tag{62}$$

$$C_2 = \frac{(\sigma_1 + \sigma_2 - 2\sigma_0 - \gamma)^2}{(\sigma_2 - 2\sigma_0)(2\sigma_0 - \sigma_1)\gamma R} \tag{63}$$

$$C = \left(1 - \frac{\sigma_1\sigma_2 - 2\sigma_0\gamma}{\sigma_0^2 + \omega_0^2}\right)\frac{1}{\gamma R} \tag{64}$$

$$R_1 = \frac{(\sigma_2 - 2\sigma_0)(2\sigma_0 - \sigma_1)\gamma R}{(\sigma_1\sigma_2 - 2\gamma\sigma_0)(\sigma_1 + \sigma_2 - 2\sigma_0 - \gamma)} \tag{65}$$

$$R_2 = \frac{\gamma R}{\sigma_1 + \sigma_2 - 2\sigma_0 - \gamma} \tag{66}$$

It should be noted that each of the quantities given by Equations 62 through 66 is in terms of the load resistance R. The factor, γ, is an arbitrary quantity which allows some flexibility in the design of the network. This quantity is subject ot the restriction given in Equation 67.

$$0 < \gamma < \frac{\sigma_1\sigma_2}{2\sigma_0} \tag{67}$$

One of the important requirements in the design is frequently the d-c gain, which is given in Equation 68.

$$T_{12}(0) = 1 - \frac{2\gamma\sigma_0}{\sigma_1\sigma_2} \tag{68}$$

Thus it may be seen from Equation 68 that a small value of γ is desirable to obtain a large value of d-c gain.

It may be shown that the capacitance, C_2, which is the largest capacitance in the network, will have its minimum value when γ has its largest value as is given in Equation 67. For this maximum value of γ, the minimum value of C_2 is given by Equation 69.

$$C_{2min} = \frac{(2\sigma_0 - \sigma_1)(\sigma_2 - 2\sigma_0)}{2\sigma_0\sigma_1\sigma_2 R} \tag{69}$$

In addition, the sum of C_1 and C is inversely proportional to γ R. Thus one has the conflicting requirements of a small value of γ for high d-c gain and a large value of γ for small capacitances. In general, some compromise must be made.

If it is possible to choose values for σ_1 and σ_2, as large value of σ_1 and as small a value of σ_2, consistent with

Equation 61, should be chosen to obtain lower values of total capacitance.

4.0 SIMPLIFICATION OF NETWORK SYNTHESIS BY BUFFER AMPLIFIERS

The availability of an ideal buffer amplifier greatly simplifies the design of networks that will synthesize a given transfer function. The reason for this is obvious if one considers the following transfer function:

$$T_{12}(s) = K \frac{(s+\sigma_1)(s+\sigma_2)(s+\sigma_3)(\overline{s+\sigma_0}^2 + \omega_o^2)}{(s+\sigma_4)(s+\sigma_5)(s+\sigma_6)(s+\sigma_7)(s+\sigma_8)} \tag{70}$$

which can be rearranged as

$$T_{12}(s) = K \underbrace{\left(\frac{s+\sigma_1}{s+\sigma_4}\right)}_{N_1} \times \underbrace{\left(\frac{s+\sigma_2}{s+\sigma_5}\right)}_{N_2} \times \underbrace{\left(\frac{s+\sigma_3}{s+\sigma_6}\right)}_{N_3} \times \underbrace{\left(\frac{\overline{s+\sigma_0}^2 + \omega_o^2}{(s+\sigma_7)(s+\sigma_8)}\right)}_{N_4} \tag{71}$$

Each individual term within a parenthesis can be developed or synthesized separately, which is a rather easy task even considering the complex zeros. The resulting network could take the form of Figure 24.

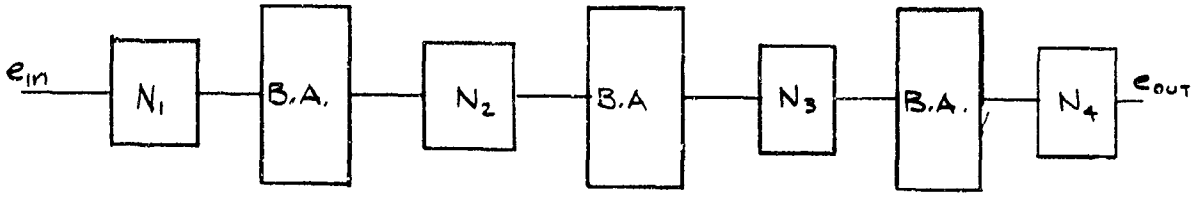


Figure 24. A Buffer Amplifier Approach to Network Synthesis

The number of buffer amplifiers could be reduced by combining two or more of the pole-zero patterns as is indicated in Equation 72.

$$T_{12}(s) = K\left[\frac{(s+\sigma_1)(s+\sigma_2)(s+\sigma_3)}{(s+\sigma_4)(s+\sigma_5)(s+\sigma_6)}\right] \times \left[\frac{s+\sigma_0^2+\omega_0^2}{(s+\sigma_7)(s+\sigma_8)}\right] \qquad (72)$$

Of course the added complexity of the first bracketed expression causes one more difficulty in synthesizing the compensating network; however, only one buffer amplifier is required in synthesizing Equation 72 as compared to three for Equation 71.

The reasons for choosing the buffer amplifier approach to network synthesis are perhaps obvious. One, it is much easier to realize a complex transfer function. This is a very important point to consider since synthesis is a trial and error process and much time can be consumed in looking for the "right" circuit. Although buffer amplifiers are relatively expensive when compared to the price of a single capacitor or resistor, a buffer amplifier can replace several passive circuit elements and save the design engineer a considerable amount of time. Two, the buffer amplifier can provide circuit gain as well as isolation. The low d-c gain of the usual circuit representing a complex transfer function can be greatly increased by one, two, or more buffer stages. In addition, the buffer amplifiers can main-

tain a higher signal level throughout the network with a resultant improvement in the signal to noise ratio.

There are, of course, some disadvantages in using buffer amplifiers such as the necessity for supplying power to the device, amplifier saturation and drift. One might also expect a bandwidth limitation but for servo applications, the amplifier bandwidth usually far exceeds the system bandwidth.

In this report the use of only one or two buffer amplifiers is considered. The buffer amplifiers are considered to be ideal; i. e., inifinite input impedance, zero output impedance, a reasonable gain 100, and a wide bandwidth. The description of the actual buffer amplifier used in this project is included in Section 6. 1.

4. 1 Use of One Buffer Amplifier

The transfer function that will be used to illustrate the buffer amplifier approach is the one which is synthesized by the UA-4 network or

$$T_{12}(s) = \left[\frac{(s+82)(s+.94)}{(s+1000)(s+1200}\right]\left[\frac{\overline{s+50}^2+130^2}{(s+2)(s+300)}\right] \qquad (73)$$

where $T_{12}(s)$ is arranged for synthesizing. In order to carry

out the synthesis procedure, refer to Section 3.2 for the first bracketed expression and Section 3.3 for the second bracketed term. First check to see that the inequality shown in Equation 42 is satisfied. As

$$0 < 82 < 184 < 1000 < 1200$$

does satisfy the inequality, simply substitute the proper values into Equations 54-58. Note that

$$a = 82 \quad b = 184 \quad c = 1000 \quad d = 1200$$

and by arbitrary choice let $R_1' = 50{,}000\ \Omega$ and $\sigma = 1100$ (σ must satisfy Equation 46 such that $1000 < \sigma < 1200$). R_1' is chosen as $50{,}000\ \Omega$ because this is assumed to be the input impedance of the amplifier following the corrective network. The resultant network that synthesizes the transfer function

$$\frac{(s+82)(s+184)}{(s+1000)(s+1200)}$$

is shown in Figure 25.

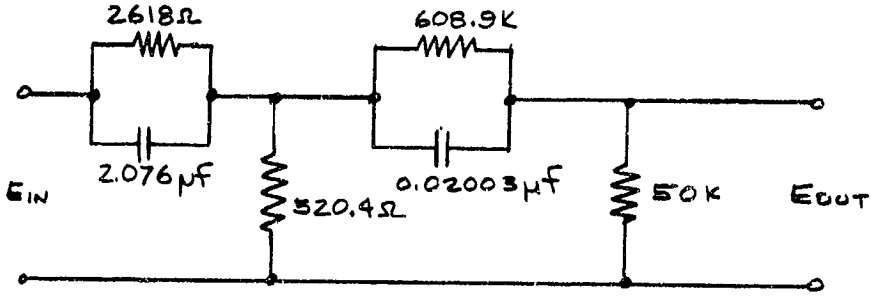


Figure 25. A Network that Synthesizes the 1st Bracketed Expression in Equation 73.

To complete the design of a network that will synthesize Equation 73, it is next necessary to concentrate on the transfer function

$$\frac{(S+50^2+130^2)}{(S+12)(S+300)}$$

which is recognized as having a complex conjugate pair of zeros and two real poles. The values of the poles and zeros meets the inequality stipulated by Equation 61 or

$$\sigma_1 < 2\sigma_0 < \sigma_2$$

$$2 < 2\times 50 < 300$$

Upon substituting

$$\sigma_0 = 50,\ \omega_0 = 130,\ \sigma_1 = 2,\ \sigma_2 = 300,\ C_2 = 10\mu f,\ R = 50K$$

into Equations 62 through 66, one obtains the specific values for the parameters of the circuit shown in Figure 21 and redrawn here as Figure 26.

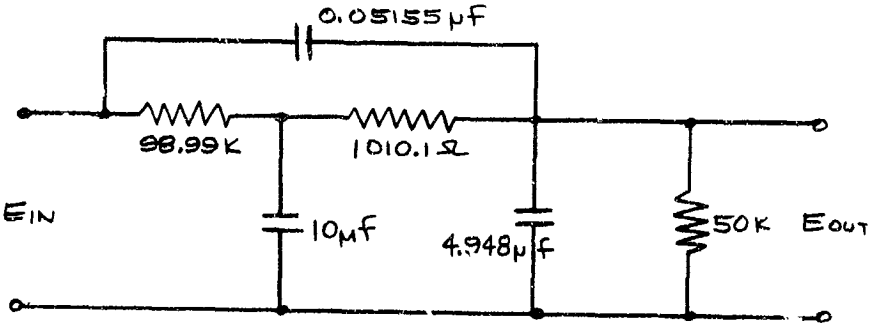


Figure 26. A network that synthesizes the 2nd bracketed expression in Equation 73.

Again the choice of R = 50,000 ohms was made on the basis of the assumed input impedance of an amplifier following the network and the value of 10 μf was chosen as the largest convenient value possible. By changing the impedance levels of the network (multiplying all resistances by a constant and dividing all capacitances by the same constant) one can obtain almost any desired maximum or minimum desired value of R or C consistent with other practical considerations such as cost, size, voltage ratings, temperature coefficients, noise generation, tolerances, and so forth.

It should be noted that the open circuit voltage transfer function of the circuit shown in Figure 26 is

$$\frac{E_{OUT}}{E_{IN}}(s) = 0.01031 \frac{\overline{s+50}^2 + 130^2}{(s+2)(s+300)} \qquad (74)$$

This means that the gain of the buffer amplifier would have to equal $\frac{1}{0.01031}$ if the transfer function of the overall network shown in Figure 27 is to exactly duplicate Equation 73.

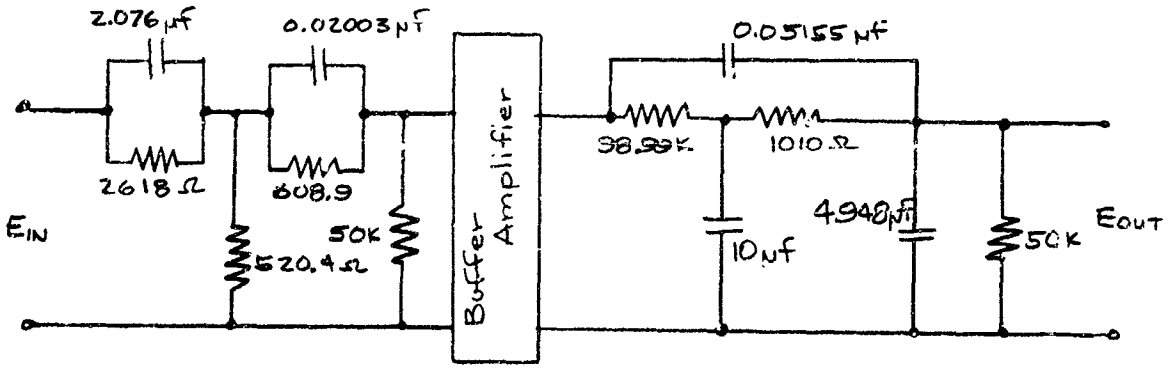


Figure 27. Overall one buffer amplifier network that combines the passive networks of Figures 25 and 26 and subject to a magnitude gain K synthesizes the equation

$$T_{12}(s) = K\frac{(s+82)(s+184)\left(s^2+50^2+130^2\right)}{(s+1000)(s+1200)(s+2)(s+300)}$$

4.2 Use of Two Buffer Amplifiers

For the transfer function given by Equation 73, the use of two buffer amplifiers is probably not justified unless one needs additional gain in the network. The only additional advantage in using two amplifiers is that the two real-zero-two real pole combinations can be synthesized by two simple R-C lead networks instead of one ladder network as shown in Figure 26. Rearranging Equation 73

$$T_{12}(s) = \frac{s+82}{s+1000} \times \frac{s^2+50^2+130^2}{(s+2)(s+300)} \times \frac{s+184}{s+1200} \qquad (75)$$

one can see that the inner equation is identical to Equation 74

and the circuit synthesizing this equation can be identical to that shown in Figure 26. Since the R-C circuits that will synthesize the transfer functions $\frac{S+82}{S+1000}$ and $\frac{S+184}{S+1200}$ are rather simple to develop, the development will not be shown here. The overall network that will synthesize Equation 75 and Equation 73 (subject to a constant gain factor) using the two buffer amplifier approach is shown in Figure 28.

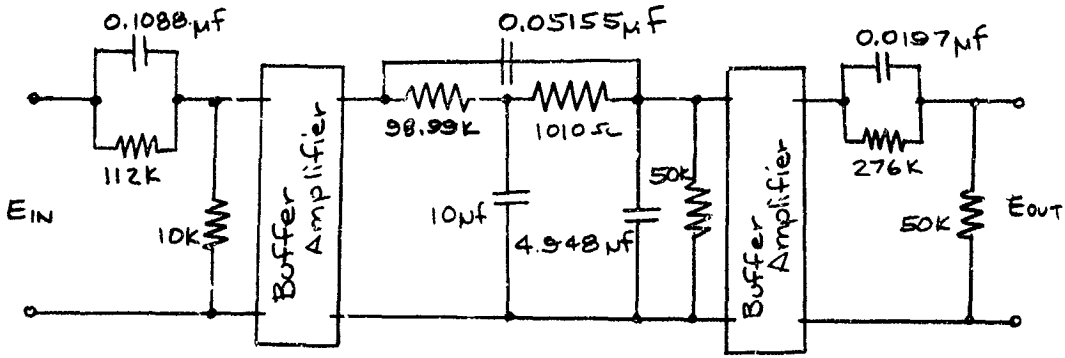


Figure 28. Overall two buffer amplifier network that synthesizes the equation

$$T_{12}(S) = \frac{S+82}{S+1000} \times \frac{\overline{S+50}^2 + 130^2}{(S+2)(S+300)} \times \frac{S+184}{S+1200}$$

5.0 THE USE OF OPERATIONAL AMPLIFIERS IN NETWORK SYNTHESIS

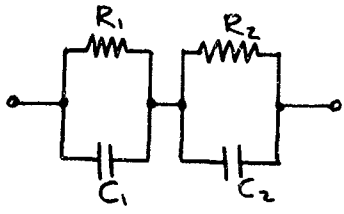
The use of high-gain direct-coupled amplifiers in synthesizing networks is most attractive. By using this approach, almost any transfer function pole-zero pattern can be synthesized. R-C, R-L or R-L-C networks can be employed as the input and feedback impedances as desired but it is to be emphasized that just R-C or R-L networks can produce complex poles as well as complex zeros in a transfer function. In addition, one can obtain a circuit gain instead of attenuation.

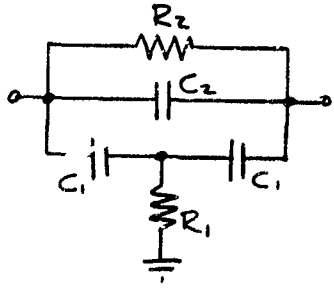
There are two general ways one can make use of the operational amplifier in synthesizing transfer functions: one, use the amplifiers in an analog computer configuration where summing, sign changing, and integrating are the only functions performed; and two, place rather complex networks in the input and feedback positions of the amplifier. The first method is simple and easy to apply but one can use a considerable number of amplifiers in a simulation. The second method requires fewer amplifiers but more ingenuity in developing the input and feedback networks. Since high-quality (high gain, high input impedance, negligible drift, temperature compensated) operational amplifiers are expensive and rather complex units, it seems desirable at present to use as few of these amplifiers as possible.

The operational amplifier approach can be illustrated by rewriting the corrective transfer function for the UA-4 system.

$$T_{12}(s) = K \frac{(s+82)(s+184)}{(s+2)(s+300)} \times \frac{\overline{s+50}^2 + 130^2}{(s+1000)(s+1200)} \qquad (76)$$

The Network





Short Circuit Transfer Impedance Function

$$A \frac{1+sT_2}{(1+sT_1)(1+sT_3)}$$

$$T_1 < T_2 < T_3$$

$$A \frac{(1+sT_3)}{(1+sT_1+s^2T_1T_2}$$

$$T_2 > \frac{T_1}{4} \text{ (complex roots)}$$

$$T_3 < T_1$$

Network Parameter Relations

$$A = R_1 + R_2 \qquad A = R_2$$

$$T_1 = R_1 C_1 \qquad T_1 = 2R_1 C_1 + R_2 C_2$$

$$T_2 = \frac{R_1 R_2}{R_1 + R_2}(C_1 + C_2) \qquad T_2 = \frac{R_1 R_2 C_1 (C_1 + 2C_2)}{2R_1 C_1 + R_2 C_2}$$

$$T_3 = R_2 C_2 \qquad T_3 = 2R_1 C_1$$

(29a) (29b)

Figure 29. Networks required to synthesize Equation 77 using operational amplifier approach.

Upon rearranging and adding some common roots

$$T_{12}(S) = \frac{A_2 \dfrac{\left(1 + \frac{S}{120}\right)}{\left(1 + \frac{S}{82}\right)\left(1 + \frac{S}{300}\right)}}{A_1 \dfrac{1 + \frac{S}{120}}{\left(1 + \frac{S}{82}\right)\left(1 + \frac{S}{300}\right)}} \times \frac{A_4 \dfrac{\left(1 + \frac{S}{1100}\right)}{\left(1 + \frac{S}{1000}\right)\left(1 + \frac{S}{1200}\right)}}{A_3 \dfrac{\left(1 + \frac{S}{1100}\right)}{\left(1 + \frac{S}{194} + \frac{S^2}{19{,}400}\right)}} \qquad (77)$$

Equation 77 places the transfer function in the proper form for synthesizing using tables of transfer impedance functions such as found in Smith and Wood.[1]

The two network configurations from Smith and Wood shown in Figure 29 are useful in synthesizing Equation 77. Figure

*1. Smith, G. W., Wood, R. C. Principles of Analog Computation, McGraw-Hill, 1959, pp. 99-101.

29a shows the network which will synthesize three of the functions of Equation 77. The network shown in Figure 29b will synthesize the remaining function

$$A_3 \frac{\left(\frac{S}{1+1100}\right)}{\left(1+\frac{S}{194}+\frac{S^2}{19{,}400}\right)} \tag{78}$$

as this function has complex poles. To illustrate the techniques the network of Figure 29b will be used to synthesize Equation 78. By comparing terms

$$T_1 = \frac{1}{194} = 2R_1C_1 + R_2C_2$$

$$T_3 = \frac{1}{1100} = 2R_1C_1$$

$$T_1T_2 = \frac{1}{19{,}400}$$

therefore

$$T_2 = \frac{1}{100} = \frac{R_1R_2C_1(C_1+2C_2)}{2R_1C_1+R_2C_2}$$

One now has three equations and four unknowns, thus one must assume a value for one of the unknwons and solve for the other three. Assuming $C_1 = 0.5\ \mu f$

$$R_1 = \frac{1}{1100 \times 2 \times 0.5 \times 10^{-6}} = 910\,\Omega$$

and from these two equations involving T_1 and T_2 one can solve for

R_2 and C_2 such that

$$R_2 = 210 \text{ K ohms}$$

$$C_2 = 0.0202 \ \mu f$$

By a similar application of Figure 29a relations and the remaining three functions in Equation 77, one can explicitly determine the necessary circuit parameters. The overall network which will synthesize Equation 77 by operational amplifiers is shown in Figure 30.

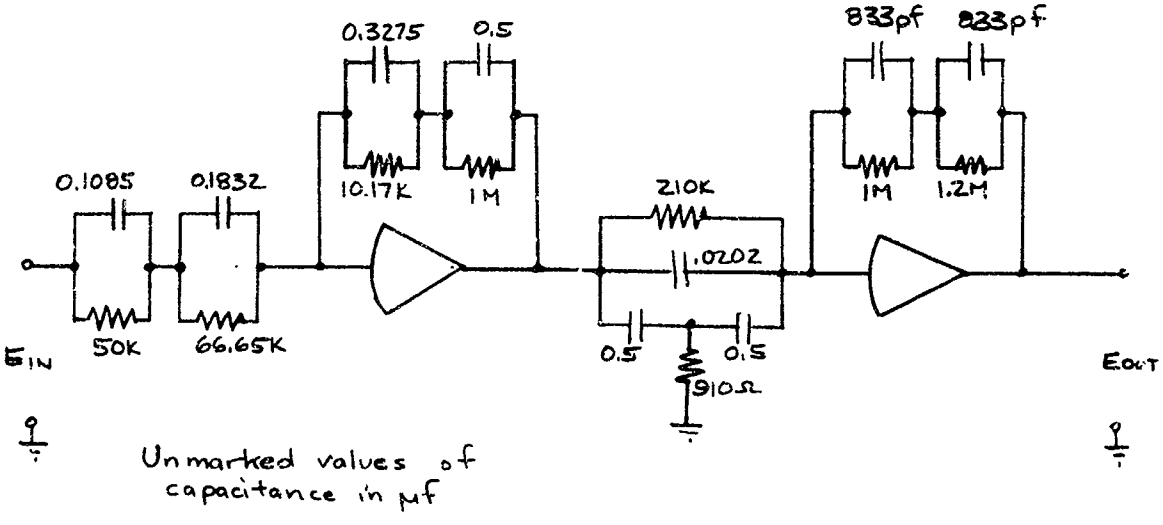


Figure 30. Operational Amplifier Approach That Will Synthesize Equation 77.

The impedance level of each of the four networks has been purposely adjusted to give a d-c gain of 10 in each operational amplifier making a total d-c gain of 100 for the overall active network.

The network shown in Figure 30 has both advantages and disadvantages over an all passive network. The disadvantages are a greater number of elements and the added cost and complexity of operational amplifiers. The advantages are relatively easy passive network design and a signal gain rather than attenuation. Since the d-c gain of the overall network is a little over 40 db, there is a gain of about 80 db over the all passive network (which has about 40 db attenuation).

For the type of transfer function as described by Equation 77, the operational amplifier approach has little or no advantage over the buffer amplifier network approach. However, for more complex transfer functions involving complex poles as well as zeros, the operational amplifier method may have decided advantages over the network using buffer amplifiers. Initial design efforts were directed toward breadboarding an operational amplifier, but because of the larger volume, power consumption and drift, work was later directed toward designing suitable buffer amplifiers.

6.0 COMPONENT STUDY

After an initial consideration of the filter networks and the functions which they would perform, it was indicated that high quality amplifiers and components would be needed. With this in mind, a limited component study was made to determine what was presently available in amplifiers and components that could be used for this application. For amplifiers, the critical specifications were input and output impedance, gain, cost, size and particularly temperature and time stability. Two general types of amplifiers were investigated. The first type was an amplifier which could be used as an operational amplifier. This in essence would be a very high performance amplifier with extremely high gain and good temperature stability. The second type considered was a buffer amplifier which could be used for isolation. The performance of this type would not be as demanding as that for the operational amplifier. For resistors and capacitors, the characteristics desired were small size, high value and good temperature stability.

6.1 Amplifiers

In order to properly choose an operational or buffer amplifier for use in network synthesis, careful attention must be given to the amplifier characteristics and the effect of these charac-

teristics on overall network parameters. Particular attention must be focused on the effect of temperature on the critical characteristics of the amplifier. Some of the more demanding characteristics and their behavior with temperature are discussed in the following paragraphs.

One of the characteristics investigated was input impedance. A high input impedance is necessary because of restrictions placed on the output impedance of the filter which would be driving the amplifiers. A high impedance level was desired because of the smaller capacitors which would be associated with it. High gain in the amplifier was desired particularly since operational amplifier gain is assumed infinite and, in the case of buffer amplifiers, the gain is used for negative feedback.

One of the most critical specifications is temperature stability or drift. For example, the circuit shown below represents the buffer amplifier and its preceeding filter.

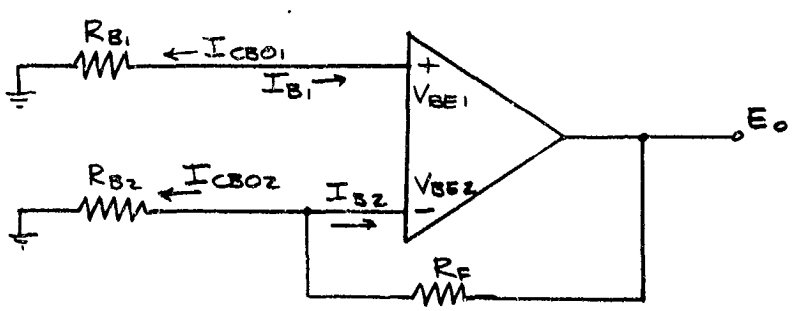


Figure 31. Representation of Isolation Amplifier

R_B1 is the output impedance of the passive filter and R_B2 is a matched impedance in the feedback circuit. Initial offset can be compensated for inside the amplifier for a particular temperature. Drift errors are caused by four principal conditions. These are: differential changes in base-emitter voltages as a function of temperature; differential changes in base currents due to differential changes in h_{fe} as a function of temperature; differential changes in I_{CBO} as a function of temperature; and differential changes in the base resistance as a function of temperature.

Therefore, the total error may be approximated as follows:

$$E = \pm(\Delta V_{BE_1} - \Delta V_{BE_2}) \pm (\Delta I_{B_1} - \Delta I_{B_2}) R_B \pm (\Delta I_{CBO_1} - \Delta I_{CBO_2}) R_B \pm (\Delta R_{B_1} - \Delta R_{B_2}) I_B \quad (79)$$

Assuming the use of a good differential input transistor for such as an Amelco 2453A with a base current of 0.1 μa, the above equation may be simplified to:

$$E = \pm 5\Delta T \pm 163(10^{-6}) R_B \Delta T \pm 531(10^{-6}) R_B \Delta T \pm 0.2\, T_c R_B \Delta T \quad \mu\text{volts}$$

where $\Delta T = T_{actual} - 25^{\circ}C$, T_c = temperature coefficient of the base resistors and R_B = the value of the base resistance. For larger value source resistors, the most significant terms are those due to differential changes in base current due to h_{fe}

and differential changes in collector to base leakage, I_{CBO}. It can be seen from the above equation that the error from certain terms is proportional to R_B; therefore, it is desirable to keep R_B as small as possible. Assuming R_B is a 1 meg wire wound resistor and a temperature change of 20°C, the maximum error on the input would be 5.15 millivolts. Table No. 2 shows a comparison of input voltage error as a function of resistance, temperature coefficients and change in temperature. This is the maximum error based on component tolerance limits and assuming that all errors are additive. Typical values would be less. Also, since this error is referred to the input of the amplifier, drift error at the output would be multiplied by the amplifier closed loop gain.

Resistor R_B		$E_1(\Delta V_{BE1}-\Delta V_{BE2})$			$E_2(\Delta I_{B1}-\Delta I_{B2})R_B$			$E_3(\Delta R_{B1}-\Delta R_{B2})I_B$			$E_4(\Delta I_{CBO1}-\Delta I_{CBO})R_L$			Total Error – μvolts		
		ΔT 20°	ΔT 40°	ΔT 60°	ΔT 20°	ΔT 40°	ΔT 60°	ΔT 20°	ΔT 40°	ΔT 60°	ΔT 20°	ΔT 40°	ΔT 60°	ΔT 20°	ΔT 40°	ΔT 60°
Carbon Composition	10K	100	200	300	33	66	99	9	18	27	16.7	55.5	180	160	330	590
	100K	100	200	300	330	660	990	90	180	270	167	555	1800	690	1400	3400
Tin Oxide	10K	100	200	300	33	66	99	2	4	6	16.7	55.5	180	153	315	570
	100K	100	200	300	330	660	990	20	40	60	167	555	1800	680	1400	3400
	1M	100	200	300	3300	6600	9900	200	400	600	1670	5550	18000	5300	13100	28800
Wire Wound	10K	100	200	300	33	66	99	.4	.8	1	16.7	55.5	180	150	310	565
	100K	100	200	300	330	660	990	4	8	10	167	555	1800	665	1370	3350
	1M	100	200	300	3300	6600	9900	40	80	100	1670	5550	18000	5150	12800	28300
	10M	100	200	300	33000	66000	99000	400	800	1000	16700	55500	180000	50000	121,000	280,000

Table No.2 Comparison of Input Voltage Errors as a Function of Base Resistance and Temperature — Values in Microvolts

6.1.1 Amplifier Availability Survey

The first component considered was the operational amplifier, both chopper stabilized and conventionally designed. The specifications necessary were very high gain (10^5 or greater), very low offset voltages ($\sim$ 10 μv, including temperature and long term stability) and small size. Specifications such as low power, cost, etc. were also considered. Amplifiers which were chopper stabilized typically had gains on the order of 10^5 to 10^6 which is satisfactory. The volumes averaged 10 cubic inches. A critical specification which all amplifiers failed was temperature stability. Typical drift with temperature was on the order of 1 to 10 $\mu v/^oC$ which would be unsatisfactory. Amplifiers considered include Fairchild, Philbrick, Rawco and others.

The next type of amplifier should have characteristics such that they could be used for low gain buffer amplifiers. Parameters needed were high open loop gain (in the order of 10^4), and good temperature stability (< 2.0 $\mu v/^oC$). The input impedance should be quite high ($> 1M$). As would be expected, the size should be smaller. The

specifications of amplifiers found, were gain in the order of 10^4 to 10^5, temperature drift in the range of 10 $\mu v/^oC$ to 100 $\mu v/^oC$, and input impedance typically in the range of 40K to 200K.

Amplifiers of this type which were investigated include those made by Fairchild, Philbrick, Nexus, Zeltex and others.

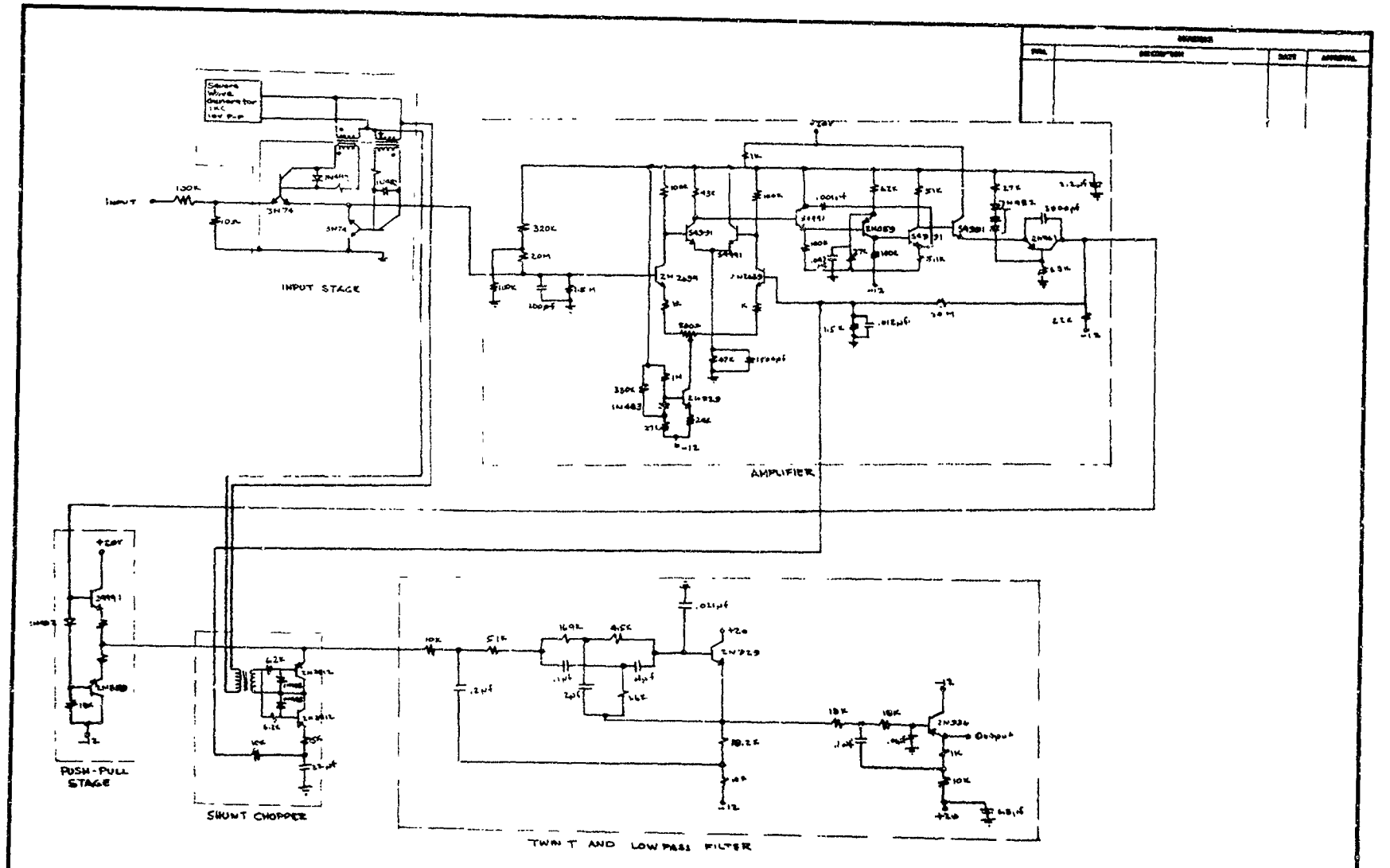
Thus, the component survey indicated that amplifiers are not readily available which would meet all the specifications for an operational amplifier in this application. This is due largely to the difficulty in applying state of the art developments to an amplifier with general specifications; i.e., not tailored to a specific application. The survey did indicate that, for the less critical buffer amplifier, there were amplifiers on the market (Nexus, Zeltex, etc.) which could be used with a small amount of additional circuitry.

6.1.2 Amplifiers Designed and Fabricated by Space Craft, Inc.

Since the parameters needed by the operational amplifier were those most unattainable, an investigation was

undertaken to determine the limiting specifications to which an amplifier of this type could be designed. A breadboard of another high performance amplifier was modified by inserting more gain stages, output filtering, and different input stages. Because the characteristics of high gain amplifiers are largely determined by the input stage, a study of various state of the art input stages would indicate to what specifications an amplifier could be designed. Various input stages were tried including shunt chopper, series-shunt chopper, and multiple differential stages. The circuit used is shown in Figure 32. This amplifier consists of a series-shunt modulator using dual emitter choppers. Following are two differential stages biased with a constant current source. Additional single ended gain stages build up the necessary amplification. This is followed by a shunt chopper demodulator. A twin T and low pass active filter removes the carrier from the output signal.

As a result of this feasibility study, it is concluded that an amplifier can be built to meet the following specifications: 0.5 $\mu v/^{\circ}C$ drift referred to the input (RTI), 8 hour stability of $\pm$ 10 μv (RTI), and less than 15 cubic inches volume. After meeting with NASA personnel and



DRAWN	LTD	Operational Amplifier Schematic Fig. 32	Space Craft Inc. Huntsville, Ala.
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reviewing the complexity of the operational amplifier and the fact that the less critical buffer amplifier and networks looked very promising, it was decided to concentrate the main effort on use of the buffer amplifier.

The second type of amplifier designed and fabricated by Space Craft, Inc. was a buffer amplifier. Even though an amplifier could have been found on the market and adapted for this purpose, it was felt that an amplifier specifically designed for this application would be superior to a modified general purpose amplifier. The resulting design which performed extremely well in the NASA accelerometer control loop is shown in Figure 33. The amplifier consists of two differential stages biased by a constant current source. They are succeeded by an emitter follower driving a common base output stage.

Characteristics of this amplifier are an open loop gain of ~14,000, a closed loop input impedance of 17M Ω, an output impedance of several ohms, and a temperature stability of less than 20 $\mu v/^{o}C$. This amplifier can be built to occupy a volume of only .5 cubic inches. A regulated power supply which will furnish power to two

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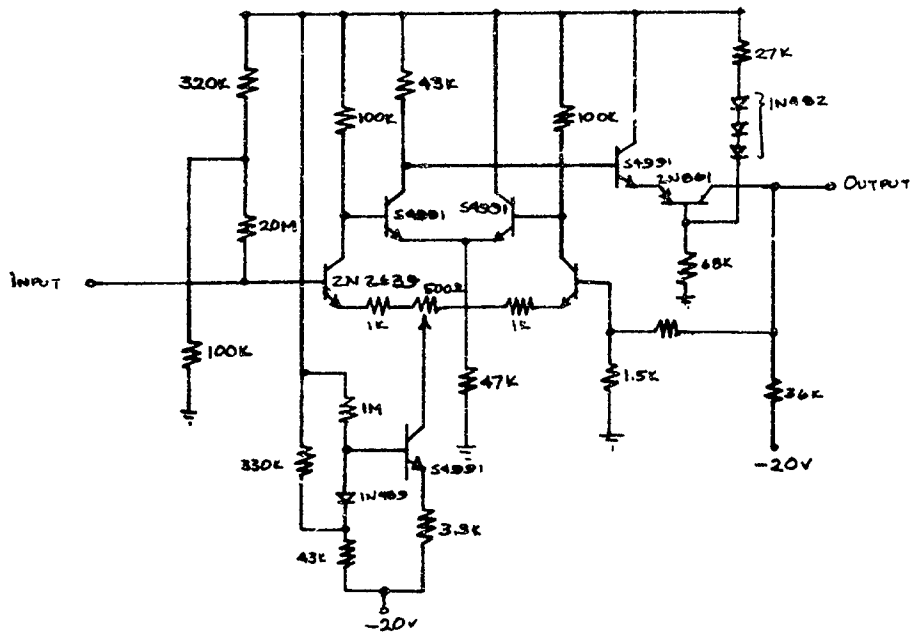

		UNLESS OTHERWISE SPECIFIED	DRAWN	JTD	Buffer Amplifier Schematic Fig. 33
		DIMENSIONS ARE IN INCHES; TOLERANCES ON: FRACTIONS DECIMALS ANGLES	DATE	3-6-64	
		MATERIAL	CHECKED	JTD	
		HEAT TREATMENT	DATE	3-6-64	
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Space Craft Inc.
Huntsville, Ala.

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of these amplifiers from a 28V supply can be built to occupy a volume of less than 1 cubic inch.

6.2 Capacitors

Capacitors represent a critical component in the various synthesis procedures used. The stringent requirements were for large values, small size and very good stability. For this reason, a survey was made to determine what was available in this range. Fortunately, a new type of capacitor began to appear on the market just as the survey began. This type is the metallized mylar and represents a ten fold improvement in volume over previous mylar capacitors. Also metalized polycarbonate capacitors offer better temperature stability but are not quite as large in value as the metalized mylar.

Three companies were found that manufacture precision small volume capacitors: Dearborn Electronic Laboratories, Inc., Box 3431, Orlando, Florida; Electron Products, 1960 Walker Avenue, Monrovia, California; and Texas Capacitor Company, 4310 Langley Road, Houston 16, Texas. The Dearborn Capacitors are metalized polycarbonate which changes with temperature less than $\pm 1\%$ from -25° to $100^{\circ}C$. They are available in values up to 5 μf with a capacitance per unit volume of 7 $\mu f/in^3$.

The Electron Products capacitors are metalized mylar. Their temperature characteristic is approximately that of plain mylar. They are available in values up to 15 μf with a capacitance per unit volume of up to 10.5 $\mu f/in^3$. The capacitors from Texas Capacitors Company are also metalized mylar. They are available in values to 20 μf, with a capacitance per unit volume of up to 20 $\mu f/in^3$. Those chosen for test were two 1 μf Texas Capacitors, one 2 μf Texas Capacitor, two 10 μf Electron Products capacitors and one 1 μf Cornell-Dublier capacitor to be used for comparison. The change in capacitance as a function of temperature was measured and the normalized resluts are shown in Table 3.

Capacitor	-20°C	0°C	20°C	40°C	60°C	80°C	% Change/°C -20°C to +85°C	0°to+40°
#1 Cornell Dublier 1μf	.991	1.000	1.000	1.001	1.006	1.025	.034	.0025
#2 Texas Capacitor 1 μf	.981	.997	1.000	1.001	1.010	1.018	.037	.010
#3 Texas Capacitor 1 μf	.986	.997	1.000	1.003	1.010	1.015	.029	.020
#4 Texas Capacitor 2 μf	.985	.997	1.000	1.002	1.008	1.023	.038	.030
#5 Electron Products 10 μf	.984	.995	1.000	1.003	1.007	1.012	.028	.012
#6 Electron Products 10 μf	.983	.992	1.000	1.004	1.004	1.013	.030	.015

TABLE 3. Normalized Change in Capacitance as a Function of Temperature

In addition to temperature characteristics, the leakage current was measured at 40 VDC and 20°C. The results of this test are presented in Table 4.

			Ic
#1	Cornell Dublier	1 μf	.1 na
#2	Texas Capacitor	1 μf	.2 na
#3	Texas Capacitor	1 μf	.2 na
#4	Texas Capacitor	2 μf	.4 na
#5	Electron Products	10 μf	2.0 na
#6	Electron Products	10 μf	2.5 na

TABLE 4. Leakage Current in Capacitors.

The tests performed by SCI on the capacitors did not, of course, constitute a complete evaluation of the samples. It did provide an indication, however, of the present state of the art in available high performance filter capacitors. The data indicated that these capacitors are well suited for the type of filters being considered.

6.3 Resistors

Resistors represent one of the less critical items

in the survey. The characteristics which are desirable in resistors are small sizes, non-standard values and good temperature stability. Numerous resistor manufacturers (Kelvin, Dale, Ultronix) make precision resistors, some with temperature coefficients as low as 2 ppm/^{o}C. These wire wound resistors may be specially made to any value from 1 ohm to about 4 meg ohm in tolerances to .01%.

7.0 CONCLUSION

In conclusion, it is believed that the development of a series of active and passive networks for stabilizing the performance of a gyro accelerometer has been satisfactorily achieved, and the primary purposes and goals of the contracted investigation have been successfully met. If the procedure of using buffer amplifiers for synthesis simplification is to be pursued further, effort directed toward development and testing of a more optimum network in the actual system would be beneficial. Some consideration should also be given toward miniaturized packaging of the amplifier and filter networks in order that they would meet the demands placed upon them by changing environmental conditions.

It was evidenced that pole placement only on the real axis did not hamper, but instead simplified, the synthesizing of networks required for stabilization. Use of bulky temperature sensitive inductors was eliminated along with the more difficult synthesis of RLC networks. Good stability and phase margins were experienced in the actual gyro accelerometer system using RC networks involving system loop gains from 5,000 to 500,000. This was a considerable improvement over the 5,000 to 7,500 loop gain being used at that time. It was discovered, however, that system stiffness increased steadily with gains

up to 25,000 but did not improve above this value. This was apparently due to noise and other less obvious factors inherent to the gyro system. Since the newly developed stabilizing networks and amplifiers exhibit very high performance, other components in the accelerometer control loop should be of equal performance in order to obtain optimum results. This is an area which was not investigated but is felt would yield improvements.

If, for some reason, it is desirable to pursue synthesizing transfer functions with complex poles, it is believed that as the state of the art progresses in new and better components, the operational amplifier approach will become increasingly more attractive.

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ABBREVIATIONS

B.S.T.J.	Bell System Technical Journal
F.I.J.	Franklin Institute Journal
IRE-AC	IRE Transactions on Automatic Control
IRE-CT	IRE Transactions on Circuit Theory
J.A.P.	Journal of Applied Physics
J.M.P.	Journal of Mathematics and Physics